Tektronix

# 数据中心的最新高速工业总线测试及SI仿真技术

Chang Yufei

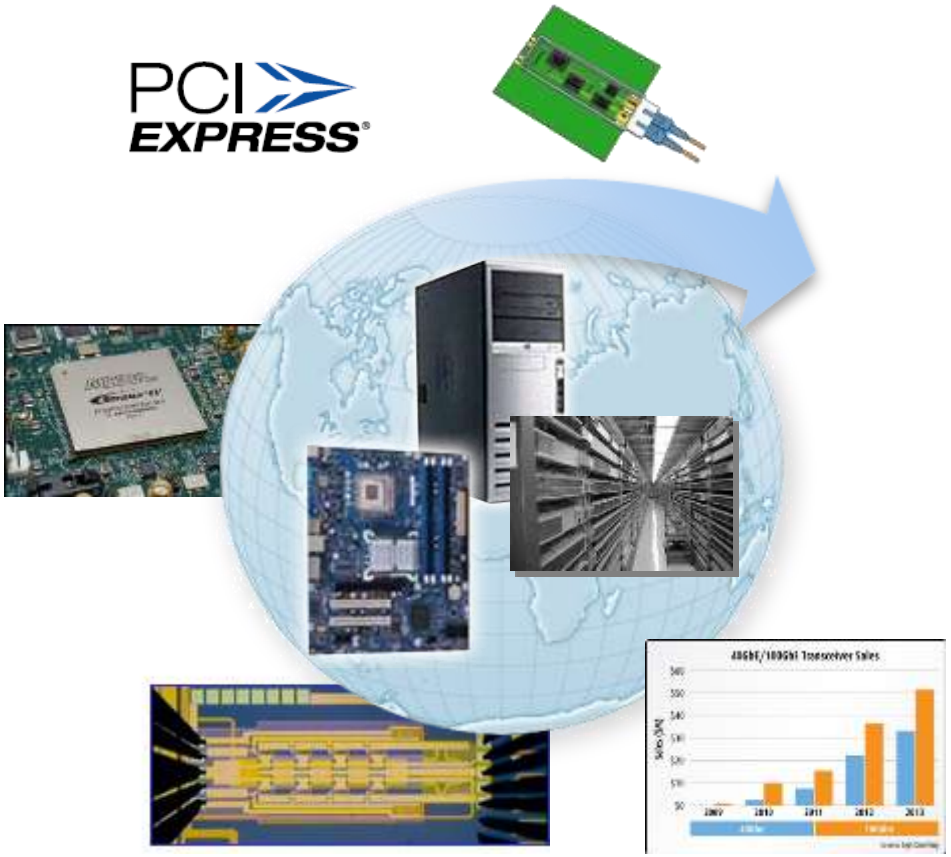
2014.4

KEITHLEY
A Tektronix Company

Tektronix

High-Speed Serial Test

# Trends and Implications




## *Industry/Technology Trends*

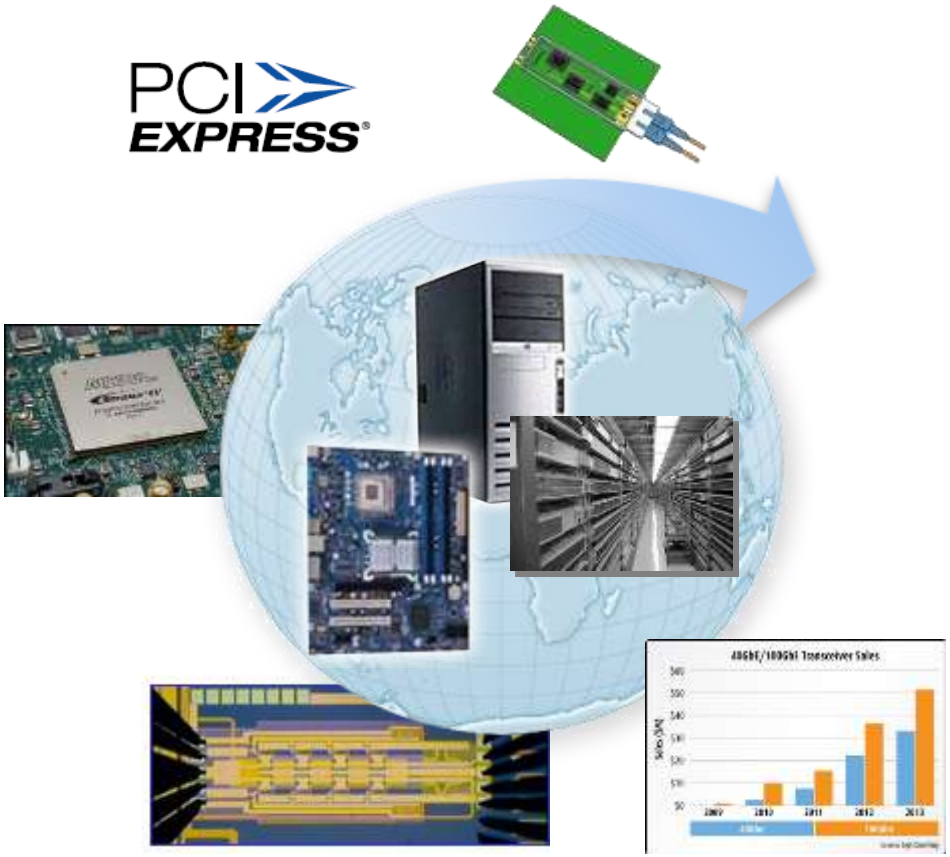
- 100 GbE is becoming more relevant as data centers and communications networks ask for more bandwidth
- SAS 12G is needed by data centers for efficient transport of internet traffic (YouTube, Facebook, Smart Phone, etc)
- High-Speed FPGA's are increasing in complexity to support early designs above 28Gb/sec
- Proliferation of 10+ Gb/sec signaling in the communications network

## *Implications*

- Closed data eyes requiring new techniques for transmitter and receiver equalization
- Higher data rate signals have less margin – requires de-embedding
- Edge/Slew rate speeds are difficult to characterize
- New Jitter Separation Measurements are required
- Complex 8b/10b signaling difficult to verify in PHY

High-Speed Serial Test

# Trends and Implications




## *Industry/Technology Trends*

- 100 GbE is becoming more relevant as data centers and communications networks ask for more bandwidth
- SAS 12G is needed by data centers for efficient transport of internet traffic (YouTube, Facebook, Smart Phone, etc)
- High-Speed FPGA's are increasing in complexity to support early designs above 28Gb/sec
- Proliferation of 10+ Gb/sec signaling in the communications network

## *Implications*

- Closed data eyes requiring new techniques for transmitter and receiver equalization
- Higher data rate signals have less margin – requires de-embedding
- Edge/Slew rate speeds are difficult to characterize
- New Jitter Separation Measurements are required
- Complex 8b/10b signaling difficult to verify in PHY

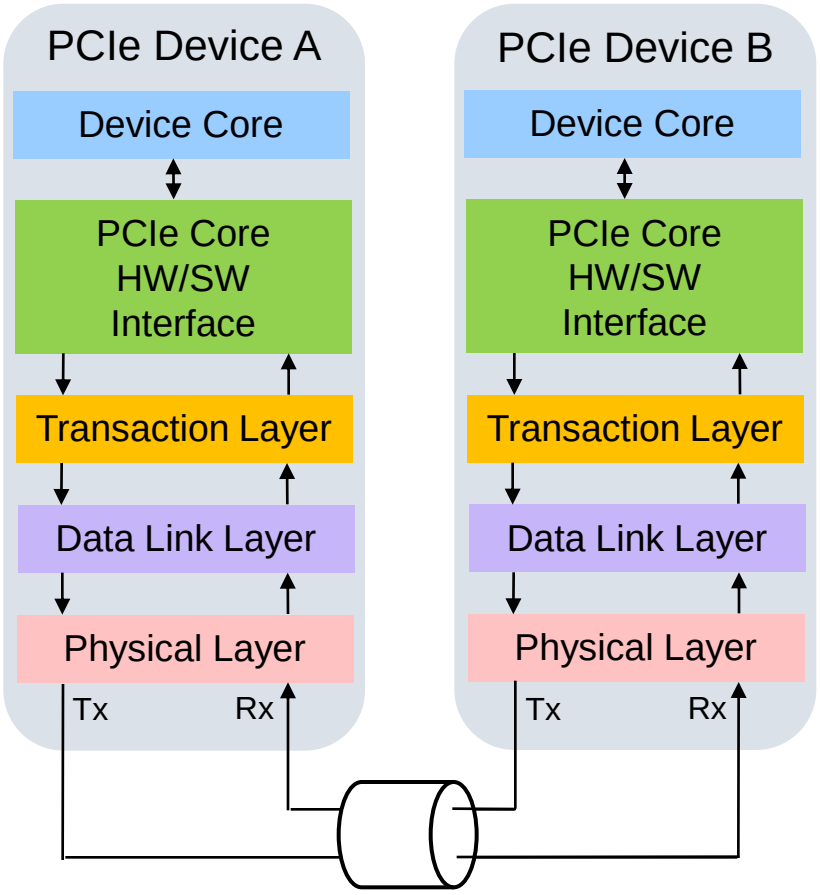
KEITHLEY
A Tektronix Company

# PCIe Gen3 Tx

KEITHLEY
A Tektronix Company

Tektronix®

# Testing Challenges with PCI Express 3.0



Logic Protocol Analyzer

Oscilloscope
Tx

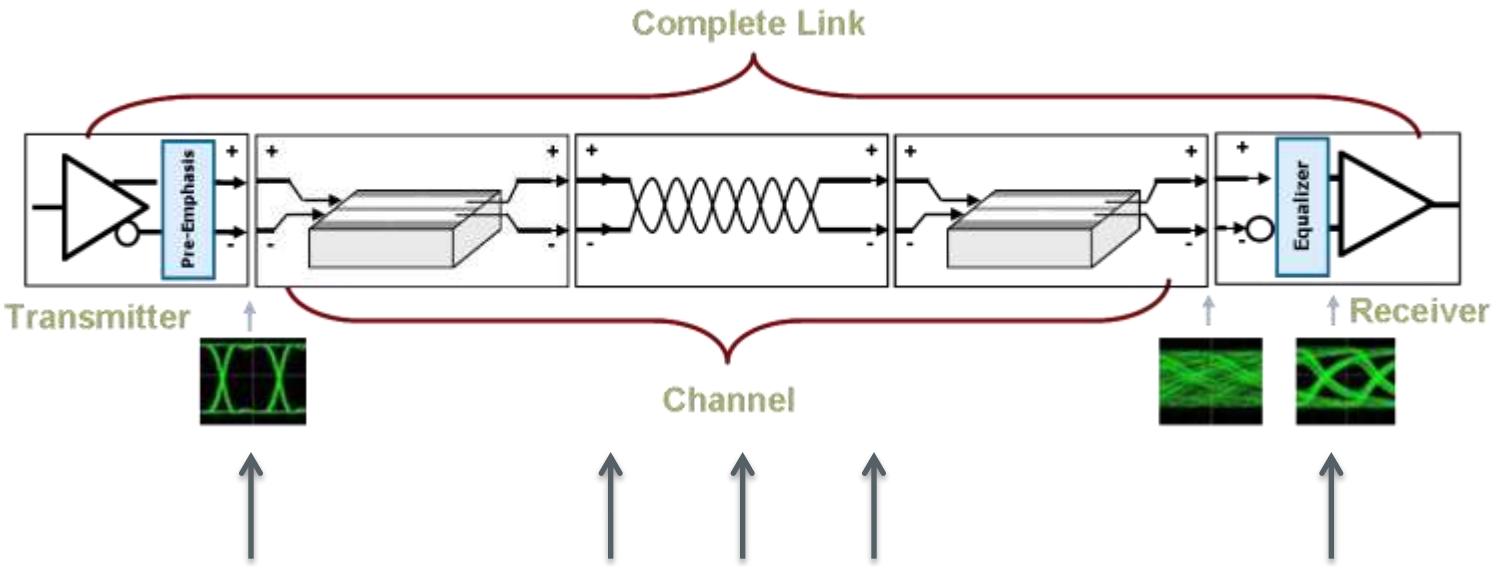
BERTScope
Rx

KEITHLEY
A Tektronix Company

Tektronix®

# PCIe Base vs CEM Testing

- What test point each type of testing addresses?
- How do we get to see the signal at the point of interest?

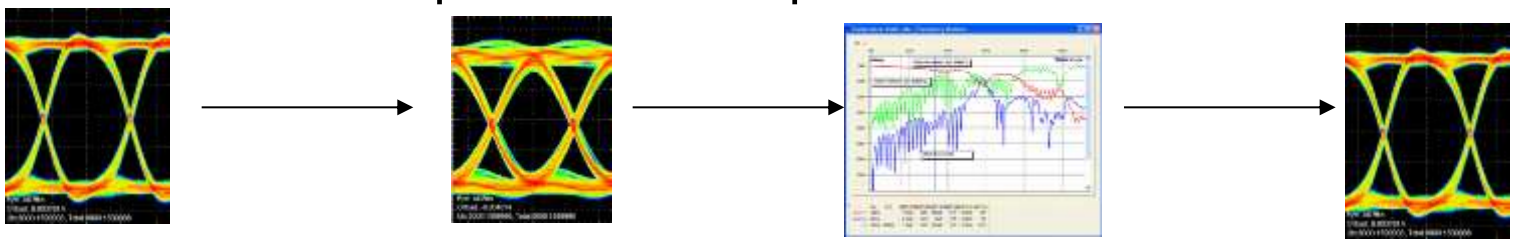




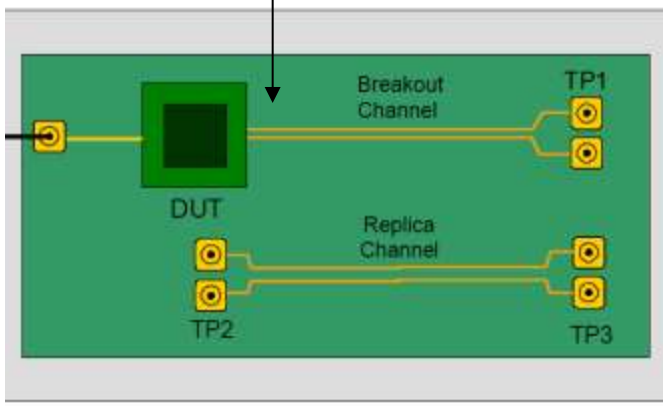
KEITHLEY
A Tektronix Company
Tektronix®

# System (Base Spec) Tx Testing

- Base Specification Measurements are defined at the pins of the transmitter
- Signal access at the pins is often not possible
- De-embedding is required to see what the signal looks like at the pins of the TX, without the added effects of the channel
- S-Parameters are acquired on the replica channel



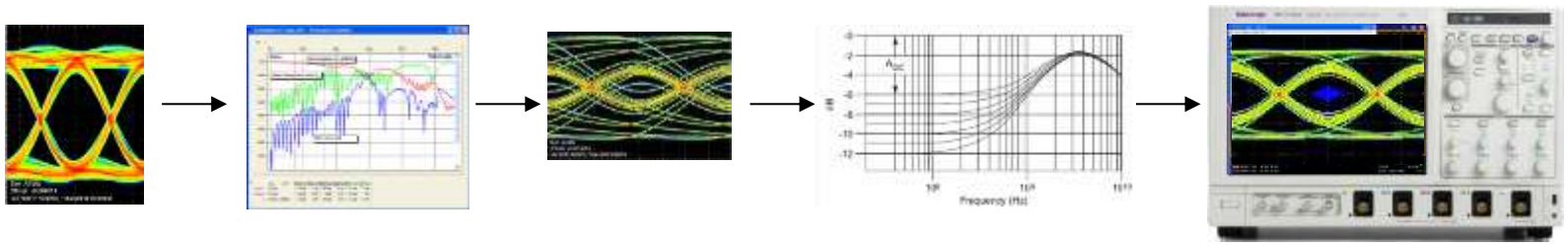
Signal at Tx Pins | Measured Signal at TP1 | De-embed using S-Parameters | Signal with Channel Effects Removed



KEITHLEY
A Tektronix Company

# Add-In Card (CEM Spec) Tx Testing

- CEM Specification Measurements are defined at the slicer of a receiver
- Signal access is not possible
- Embedding of the compliance channel and package, as well as application of the behavioral equalizer is required
- SigTest or custom software like DPOJET will perform the embedding and calculate measurements



**Signal Acquired from Compliance Board**

**Embed Compliance Channel and Package**

**Closed Eye due to the Channel**

**Apply CTLE + DFE**

**Open Eye for Measurements**

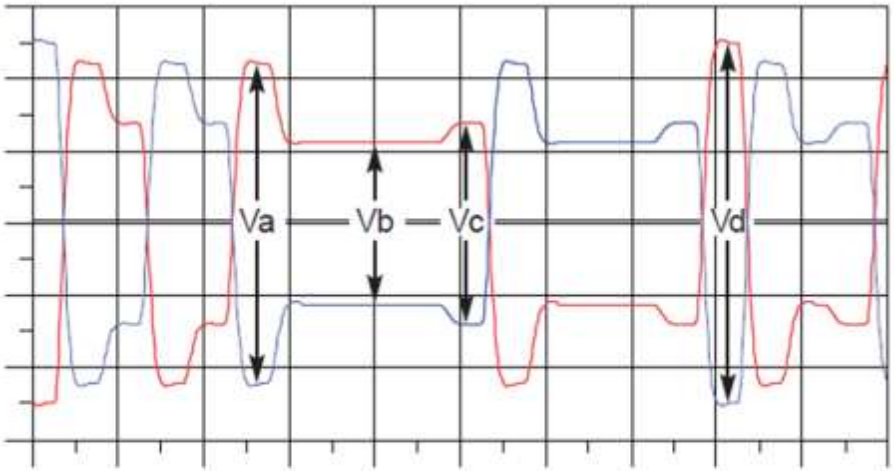
KEITHLEY
A Tektronix Company

Tektronix®

# Compliance Patterns

- Once in compliance mode, bursts of 100MHz clock can used to cycle through various settings of compliance patterns to perform, Jitter, voltage, timing measurements.

| Data Rate | Preshoot | De-emphasis |
|---|---|---|
| 2.5 GT/s, | | -3.5 dB |
| 5.0 GT/s, | | -3.5 dB |
| 5.0 GT/s, | | -6.0 dB |
| 8.0 GT/s, | P0 = 0.0 | -6.0±1.5dB |
| 8.0 GT/s, | P1 = 0.0 | -3.5±1.5dB |
| 8.0 GT/s, | P2 = 0.0 | -4.4±1.5dB |
| 8.0 GT/s, | P3 = 0.0 | -2.5±1dB |
| 8.0 GT/s, | P4 = 0.0 | 0.0dB |
| 8.0 GT/s, | P5 = 1.9±1dB | 0.0dB |
| 8.0 GT/s, | P6 = 1.9±1dB | 0.0dB |
| 8.0 GT/s, | P7 = 1.9±1dB | -6.0±1.5dB |
| 8.0 GT/s, | P8 = 1.9±1dB | -3.5±1dB |
| 8.0 GT/s, | P9 = 1.9±1dB | 0.0dB |
| 8.0 GT/s, | P10 = 1.9±1dB | Test Max Boost Limit |

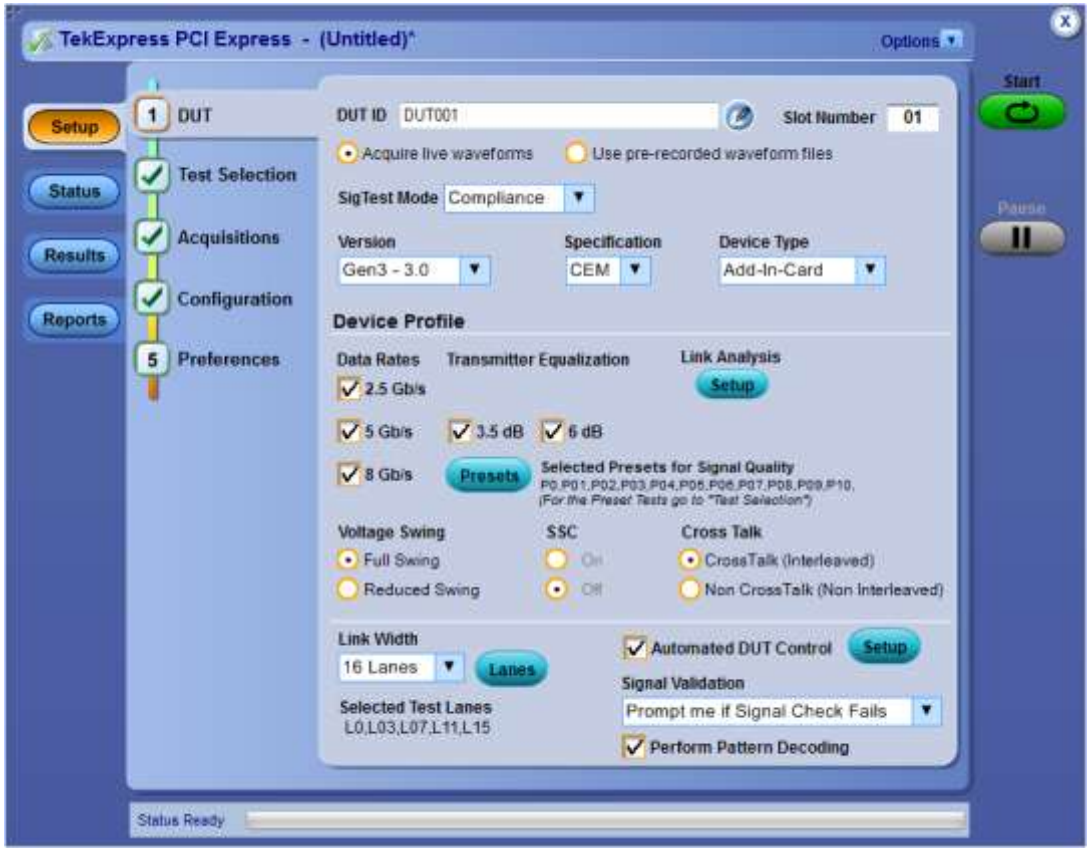


# Testing Challenges in Tx

- Meet the requirements for effective testing
  - √ Compliance mode support, proper patterns and toggling mechanism
  - √ Correct Tx equalization settings and preset and Lane ID encoding in Tx compliance pattern
- Why so many presets? How to capture so many lanes?
  - √ The answer is test automation, RF switch
- Measurement algorithms
  - √ Implemented in SigTest, or scope specific software
- How to achieve required confidence level and beyond?
  - √ Length and number of waveforms (for Tx)

# Introducing the NEW Opt PCE3

- TekExpress Automation for Tx Compliance with unique features including:
  - √ Sets up the Scope and DUT for testing
  - √ Toggles thru and verifies the different Presets and Bit Rates
  - √ Tests multiple slots and lanes
  - √ Acquires the data
  - √ Processed with PCI-SIG SigTest
  - √ Provides custom reporting




KEITHLEY
A Tektronix Company

Tektronix®

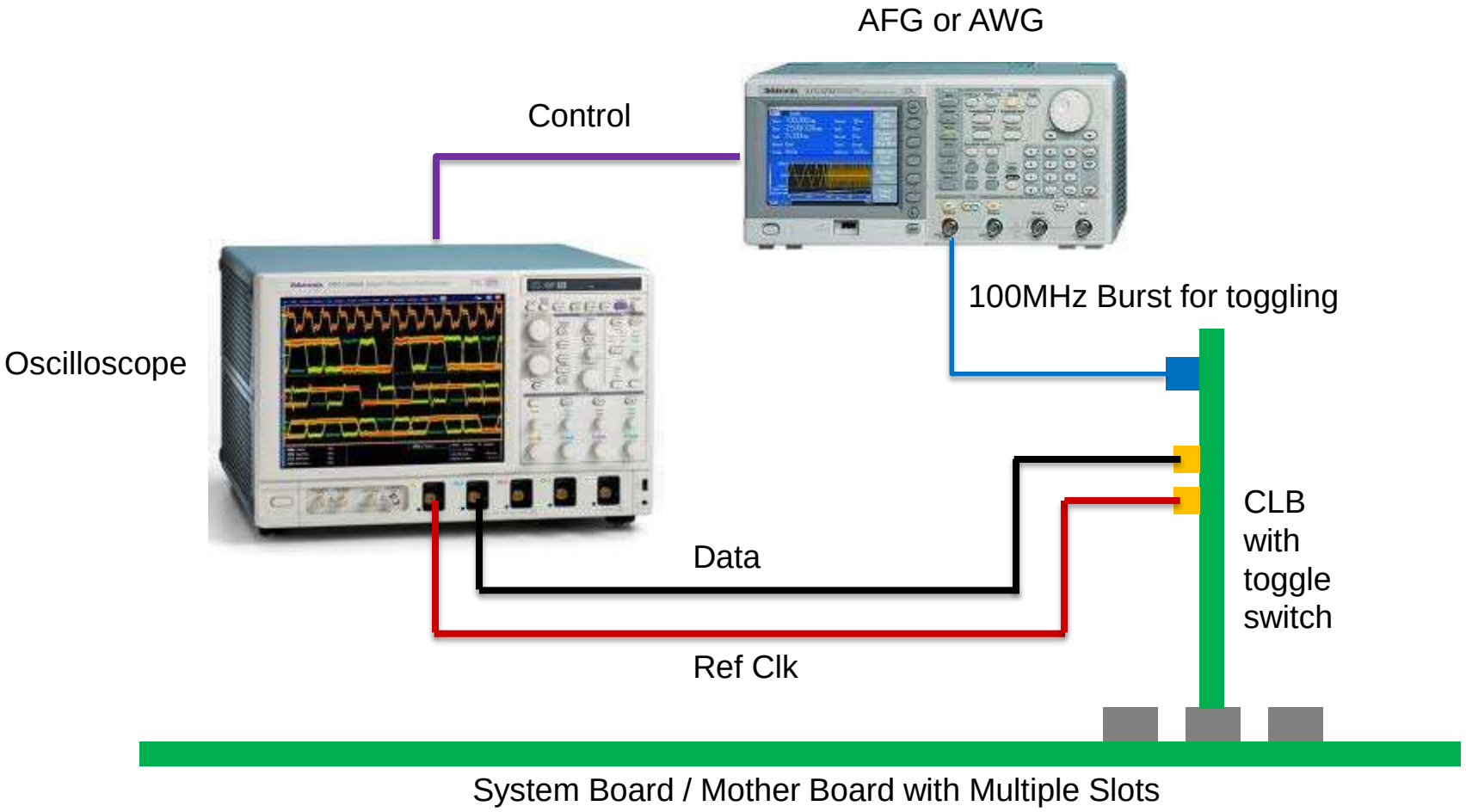
# What's New in Option PCE3 Release 2?

- Supports a faster, Python-based sequencer
  - Much faster program launch with the test time reduced by ~50%
  - 64-bit only application (requires 70K C/D oscilloscopes with Win7 64-bit)
    - Will maintain earlier 32-bit release for 70K A/B oscilloscopes with WinXP 32-bit on www.tek.com
  - Smaller installer
- SigTest.exe (Command-Line) integration
  - Supports PCI-SIG recommended SigTest.exe testing
  - User can switch between DLL and Command-Line (.exe) modes
  - All result are populated in Tektronix result/report format in command line mode
- Support multiple versions of SigTest
  - User option to select required version and run
  - Broader AWG/AFG support for automatic DUT toggle *(Min 2ch & 100MHz Burst mode)*
  - AFG3252/C
  - AWG5002B/C, AWG5012B/C, AWG5014B/C
  - AWG7082B/C, AWG7122B/C
  - AWG70001A/2A
- Incorporates customer & field feedback
  - Crosstalk option is added
  - Gen2 System-Board limit issue fixed
  - Addresses 6 customer-reported issues & ~30 PCIe Workshop-reported issues

# Automation Simplifies Tx Testing

- While convenient single capture capability is essential, automation makes the testing practical
- Iterate over multiple presets and lanes
- Gather results in a single report
- Provide means for quick switch to debugging and additional measurements
- Remove test fixture effects by using de-embedding

# Automated DUT Control



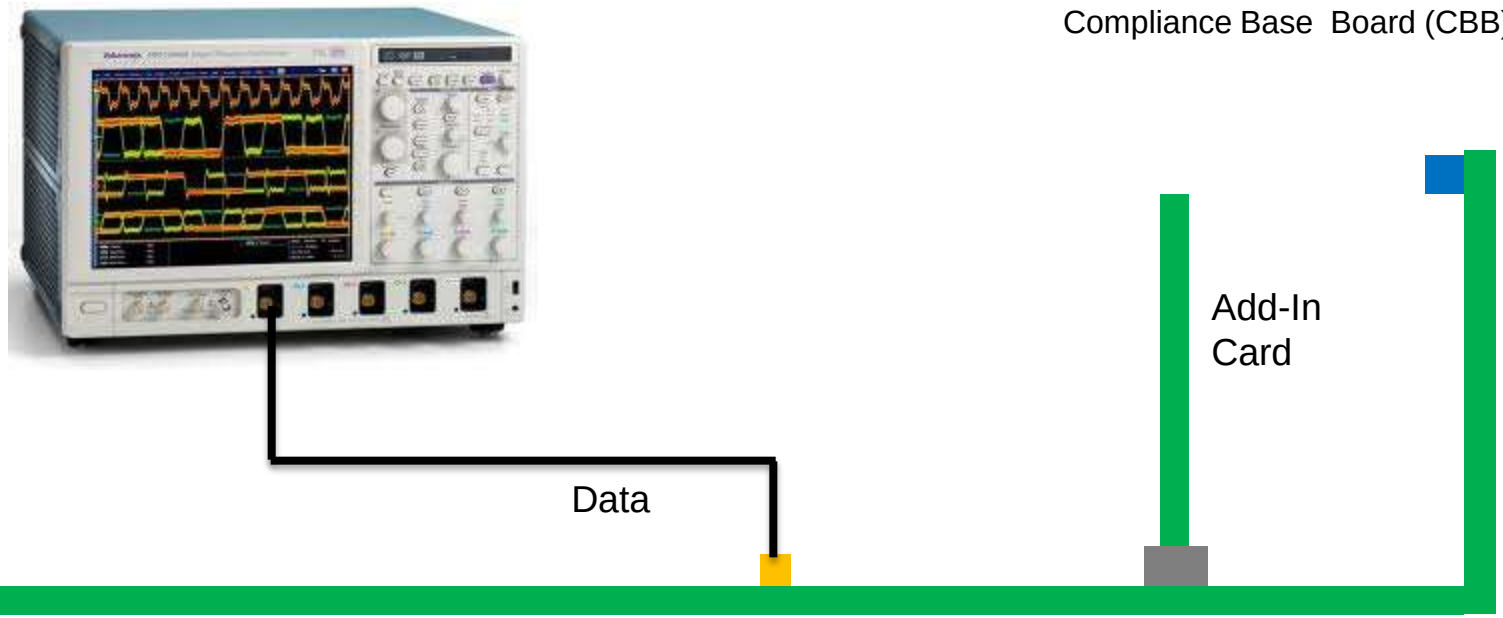

KEITHLEY
A Tektronix Company

Tektronix®

# Add-In Card Test Fixture

- Compliance Base Board (CBB)
  - Used for Testing Add-In cards
  - All Tx / Rx Lanes are routed to SMP
  - Compliance Mode Toggle Switch
  - Low Jitter Clean Reference Clock
  - Separate CBB for Gen 1/2/3

Compliance Base Board (CBB)




CBB with Multiple Slots of different widths and toggle switch

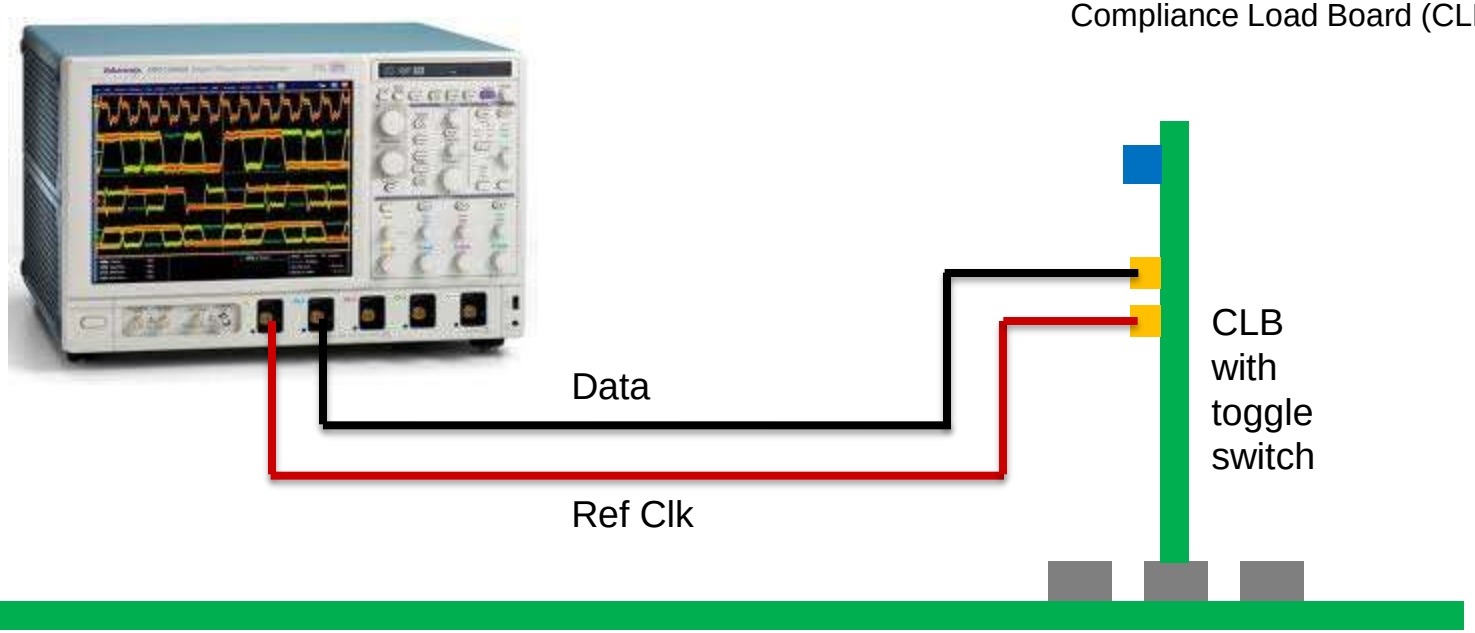
KEITHLEY
A Tektronix Company

Tektronix®

# System Test Fixtures

- Compliance Load Board (CLB)
  - Used for testing System Boards
  - All Tx / Rx Lanes and Ref Clk routed to SMP
  - Compliance Mode Toggle Switch
  - Various types of Edge Connectors to support different types of Slots on System Boards
  - Separate CLB's for Gen1/2/3

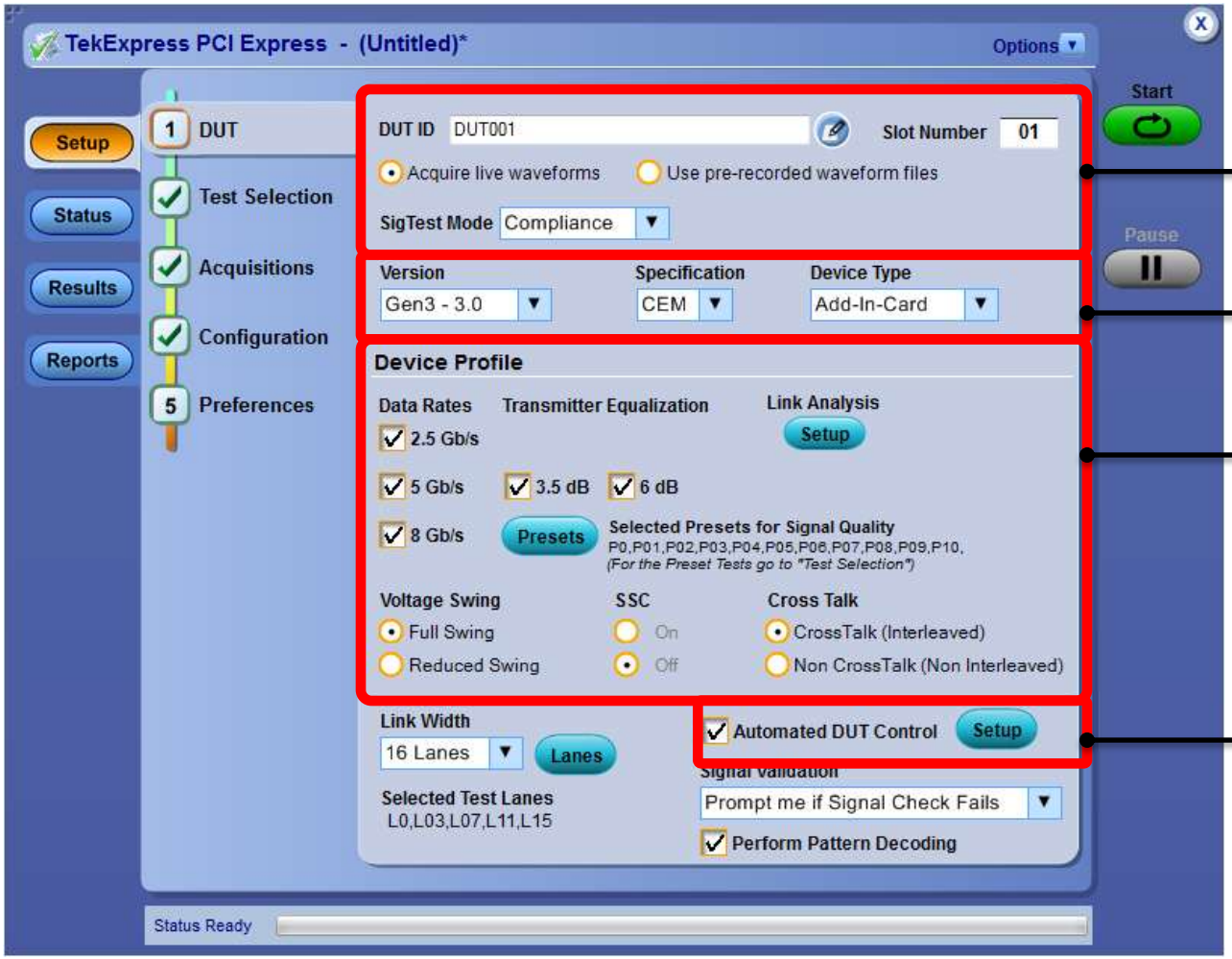
Compliance Load Board (CLB)




KEITHLEY
A Tektronix Company

Tektronix®

# TekExpress Automation for Tx Compliance - Setup




Run Analysis on Live or Pre-Recorded Data

Type of test / device selection

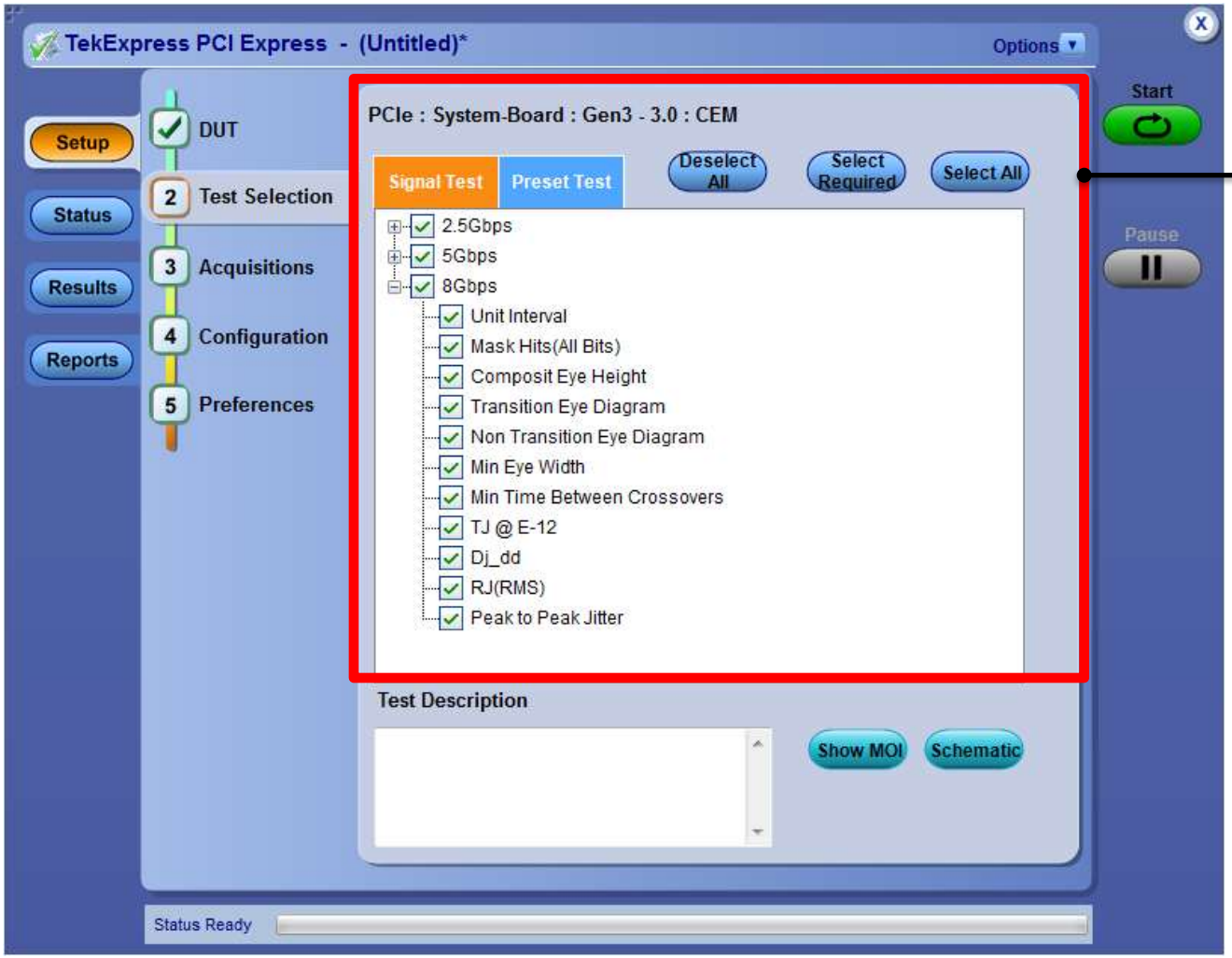
Test selection

Automate DUT control

KEITHLEY
A Tektronix Company

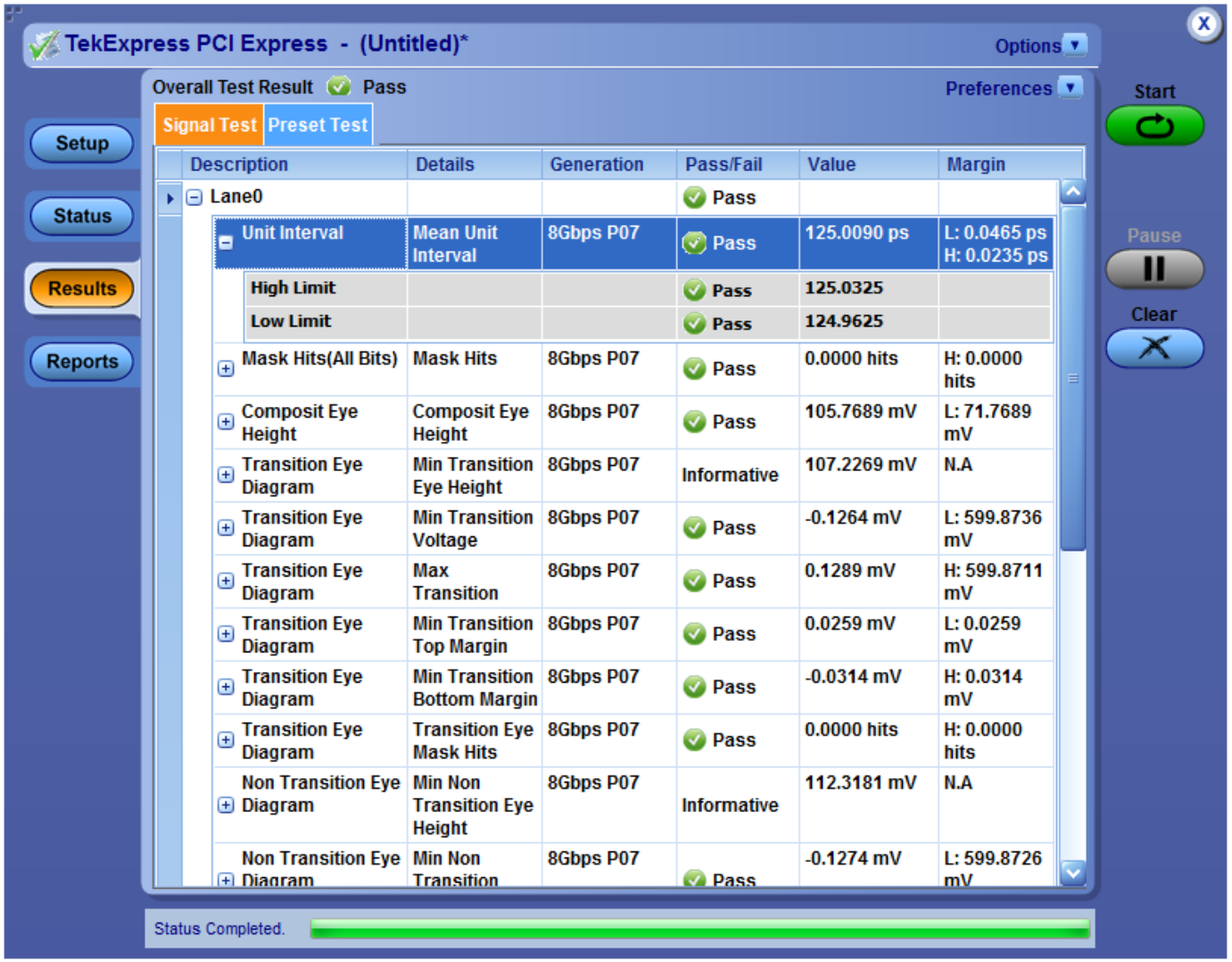
Tektronix

# TekExpress Automation for Tx Compliance – Test




**Test Selection**

# TekExpress Automation for Tx Compliance – Reports

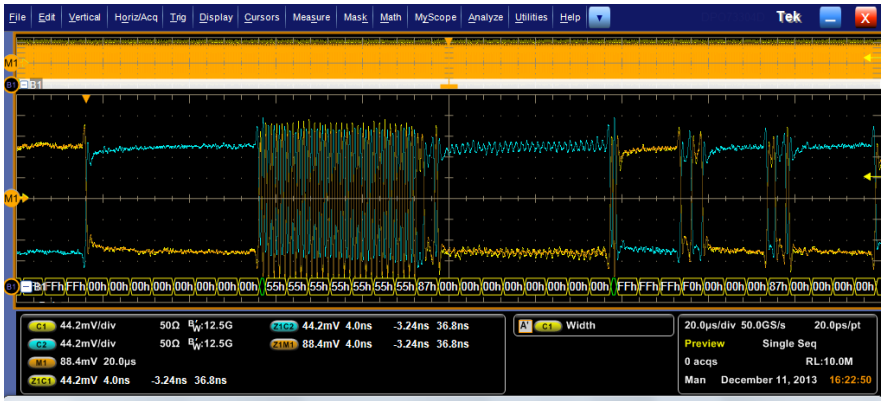


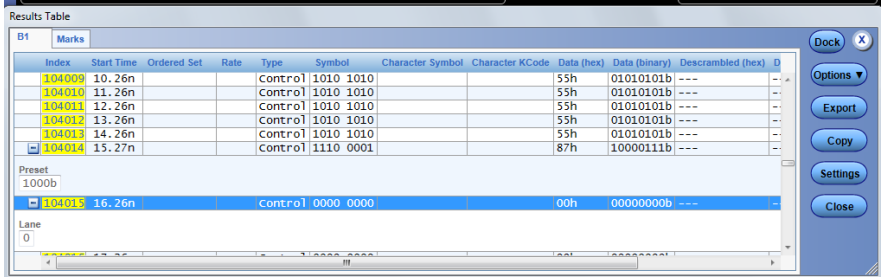

KEITHLEY
A Tektronix Company

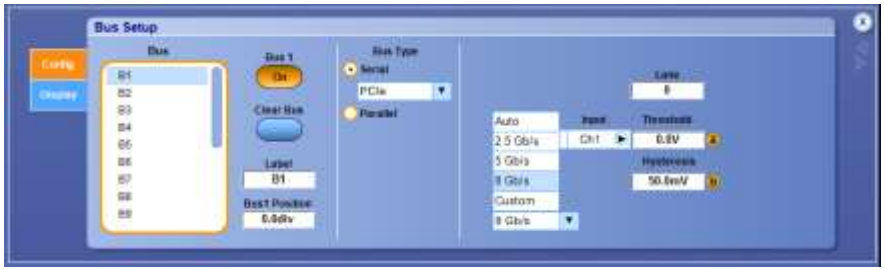
Tektronix®

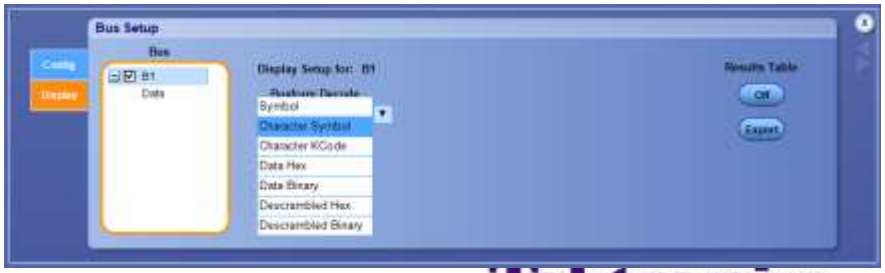
# PCIe Decoder (Opt SR-PCIe)

- Decodes and displays PCIe data using characters and names that are familiar from the standard, such as:
  - SKP
  - Electrical Idle
  - EIEOS
- Easily configured through “Bus Setup” under “Vertical” menu with a variety of user-adjustable settings
- Results table shows time-correlated listing of events time-correlated with waveform view
- Integrated search with marks
- Triggering up to 6.25Gbs (Gen1 & Gen2 only)



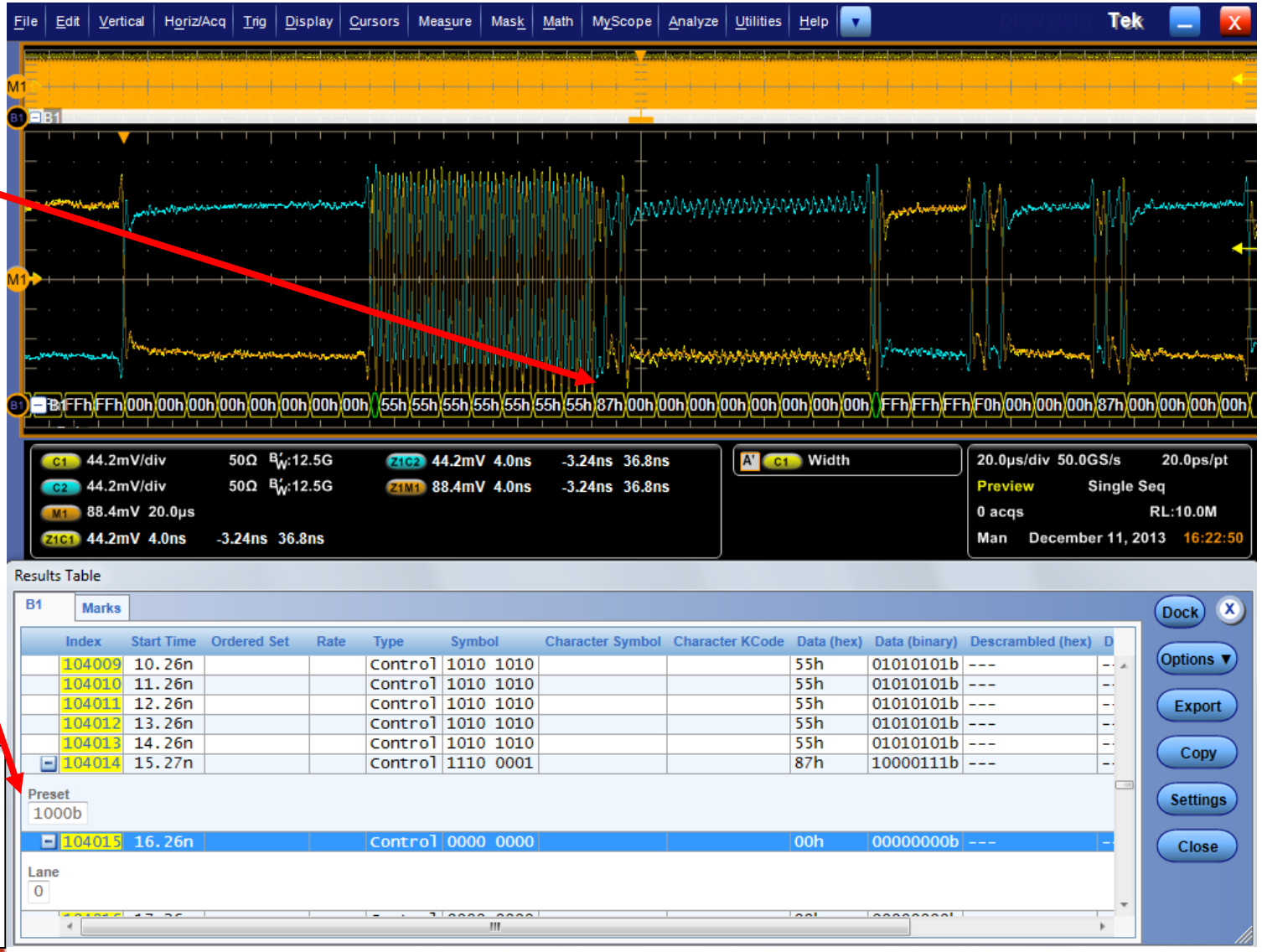

KEITHLEY
A Tektronix Company

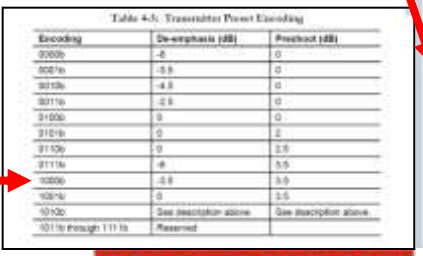
Tektronix®

# PCIe Decoder (Opt SR-PCIe)

*Decoding of PCIe Gen3 compliance pattern Tx preset encoding*

Decode results show correct value of “87h” or “1000b” (as shown in Results Table) for Transmitter Preset **P8** (-3.5dB de-emphasis with +3.5dB preshoot) on Lane 0


File Edit Vertical Horiz/Acq Trig Display Cursors Measure Mask Math MyScope Analyze Utilities Help
Tek
C1 44.2mV/div 50Ω BW:12.5G
C2 44.2mV/div 50Ω BW:12.5G
M1 88.4mV 20.0µs
Z1C1 44.2mV 4.0ns -3.24ns 36.8ns
Z1C2 44.2mV 4.0ns -3.24ns 36.8ns
Z1M1 88.4mV 4.0ns -3.24ns 36.8ns
A' C1 Width
20.0µs/div 50.0GS/s 20.0ps/pt
Preview Single Seq
0 acqs RL:10.0M
Man December 11, 2013 16:22:50
Results Table
B1
Marks
Dock
Options
Export
Copy
Settings
Close
Index Start Time Ordered Set Rate Type Symbol Character Symbol Character KCode Data (hex) Data (binary) Descrambled (hex)
104009 10.26n Control 1010 1010 55h 01010101b ---
104010 11.26n Control 1010 1010 55h 01010101b ---
104011 12.26n Control 1010 1010 55h 01010101b ---
104012 13.26n Control 1010 1010 55h 01010101b ---
104013 14.26n Control 1010 1010 55h 01010101b ---
104014 15.27n Control 1110 0001 87h 10000111b ---
Preset
1000b
104015 16.26n Control 0000 0000 00h 00000000b ---
Lane
0

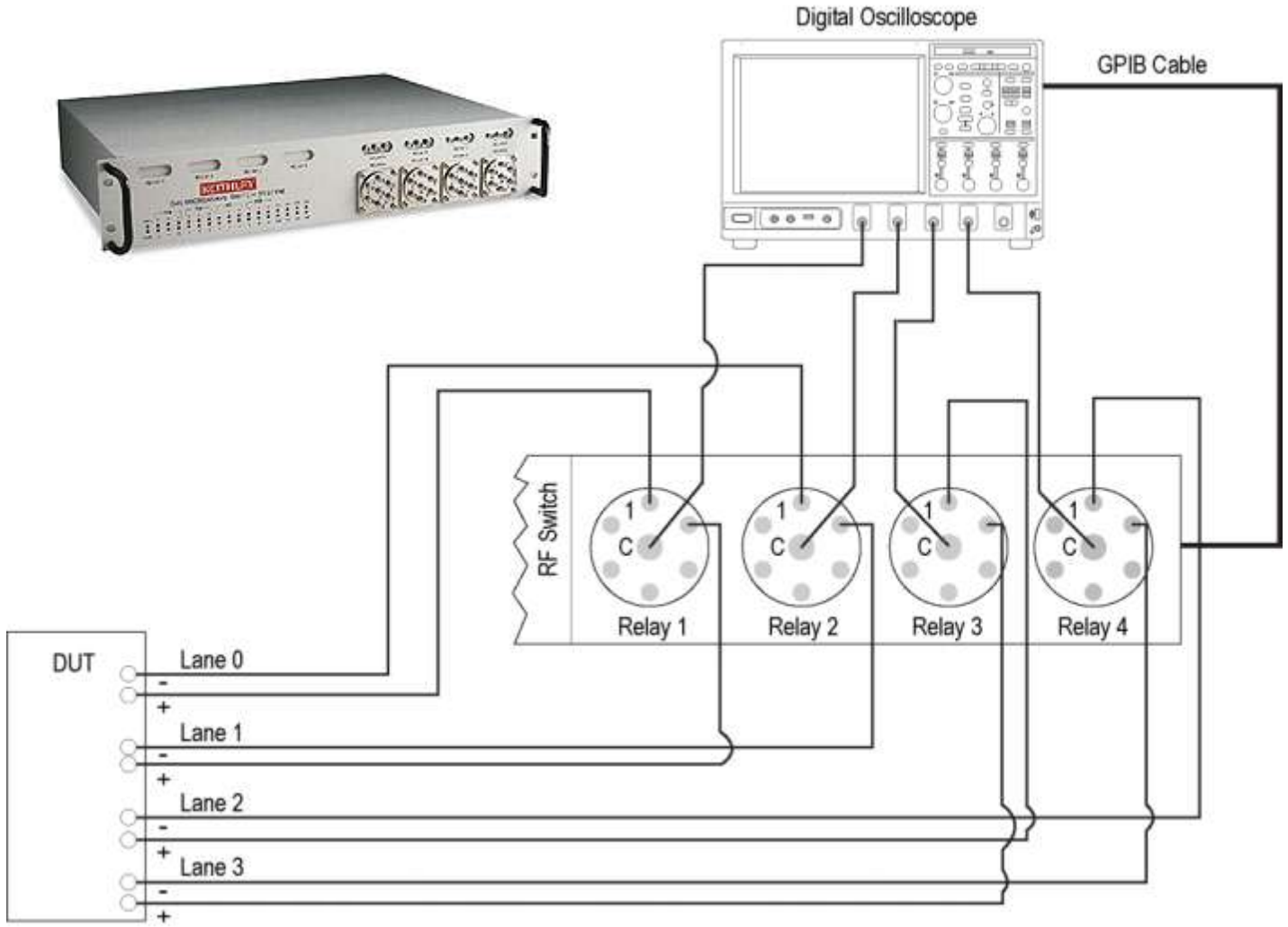


Reference: PCI Express Base Spec, Rev 3.0 (10-NOV-2010), Section 4.2.3.2 Encoding of Presets, p.225.

# RF Switch and Auto Toggling

- Use RF switch to handle multiple lanes without reconnections
  - √ Must provide termination to maintain compliance mode
  - √ Use programmatic interface to control from automation software
  - √ While switches typically have good signal quality at 4GHz, extra cables must be accounted for by de-embedding
  - √ Design you device so that automatic toggling works for all presets

# PCI Express Tx Test with RF Switch




KEITHLEY
A Tektronix Company

Tektronix®

# Cable and RF Switch De-embed

KEITHLEY
A Tektronix Company

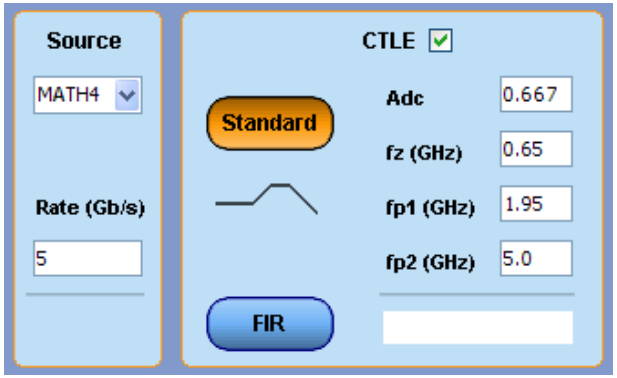
Tektronix®

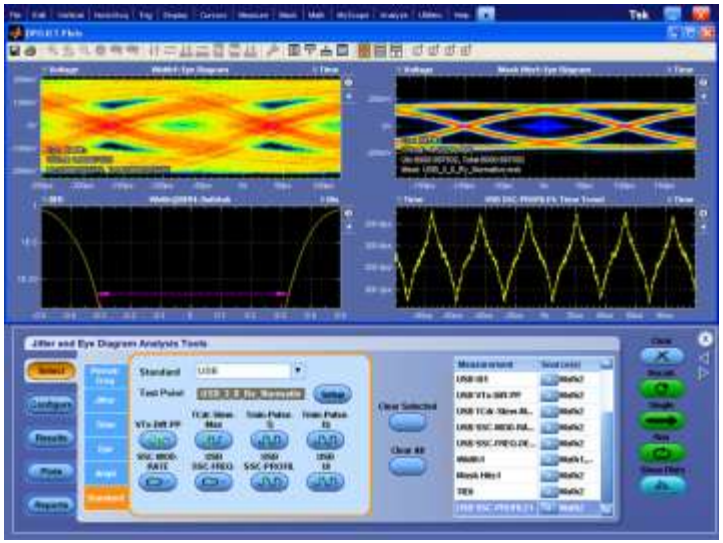
# Comparison of De-embedding: System

| System Board (P7) | With de-embed | Without de-embed | Diff |
|---|---|---|---|
| SigTest Measurement | Switch & extra cable effects removed | Switch and cable effects present | |
| Max Peak to Peak Jitter | 42.614ps | 41.619ps | 2.39% |
| Minimum eye width | 81.566ps | 82.443ps | -1.06% |
| Deterministic Jitter d-d | 31.261ps | 31.653ps | -1.24% |
| Random Jitter | 0.865ps | 0.775ps | 11.61% |
| Composit Eye height | 0.132V | 0.129V | 2.33% |
| Min Transition Eye Height | 0.165V | 0.152V | 8.55% |
| Min Non-transition Eye Height | 0.141V | 0.134V | 5.22% |

# Testing Beyond Compliance

- What happens if a measurement fails Compliance ?
- Could it be the channel?
  - Measurements can be taken before the channel to evaluate results
  - Different channel models can be created using SDLA Visualizer
- How does the optimized RX setting compare to other settings?
  - Easily compare the results of multiple Equalization settings
- Does deeper analysis of the waveform need to be done?
  - PCIe specific measurements can be taken in Tektronix' measurement system DPOJET
  - Determine if data dependent, uncorrelated or pulse width jitter is in spec
  - Measurements filters and settings can be adjusted to get to root cause, but remember you must pass SigTest to be certified for compliance
- Is the TX compliant?
  - NEW PCIe 3.0 base spec measurements are available to verify Tx compliance



KEITHLEY
A Tektronix Company

Tektronix®

# PCIe Gen3 Rx Solution

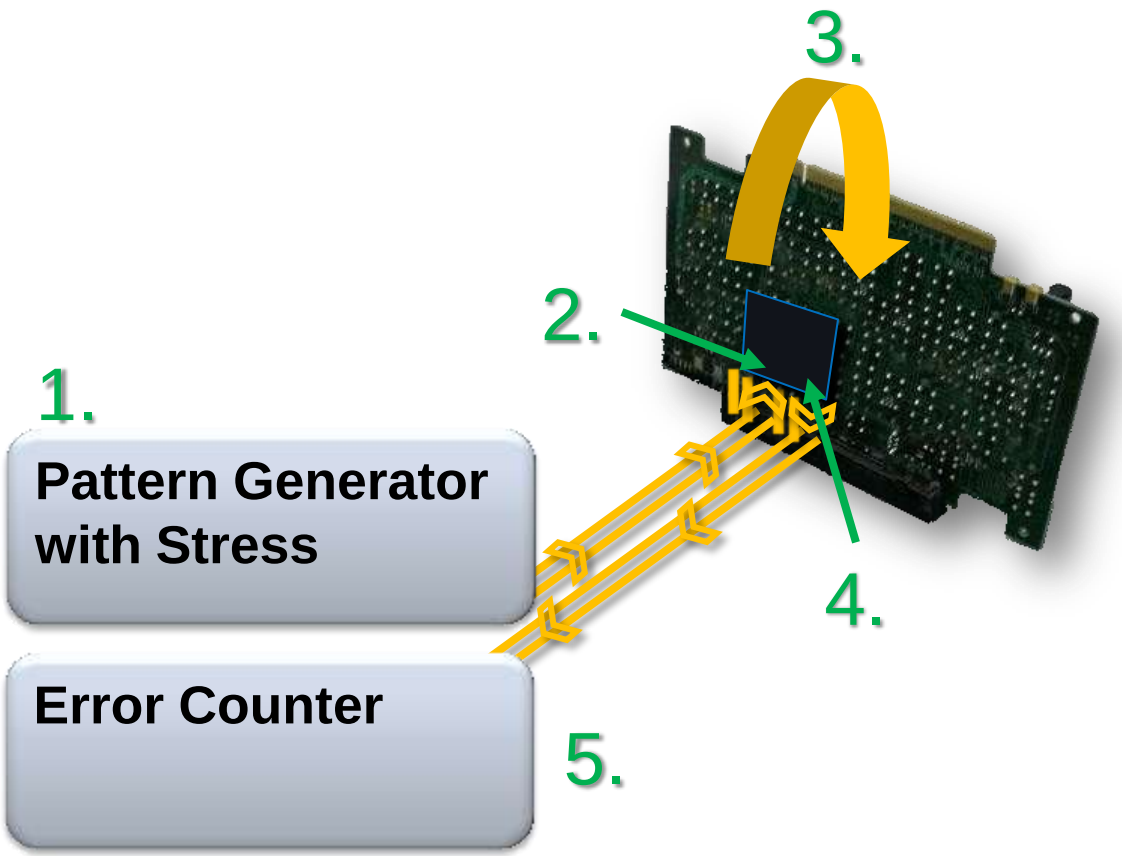
KEITHLEY
A Tektronix Company

Tektronix®

# Essentials of Rx Testing

- PCIe 3.0 introduced formal Rx testing
- Based on stress testing of the DUT in loopback
  - Looped back data must be the same as stressed data
- DUT must support loopback initialization and **training**
- Impairments in stress must be **controlled** and **repeatable**
- DUT must receive stressed signals without errors (errors below specified ratio $10^{-12}$)

# Basic Receiver Testing



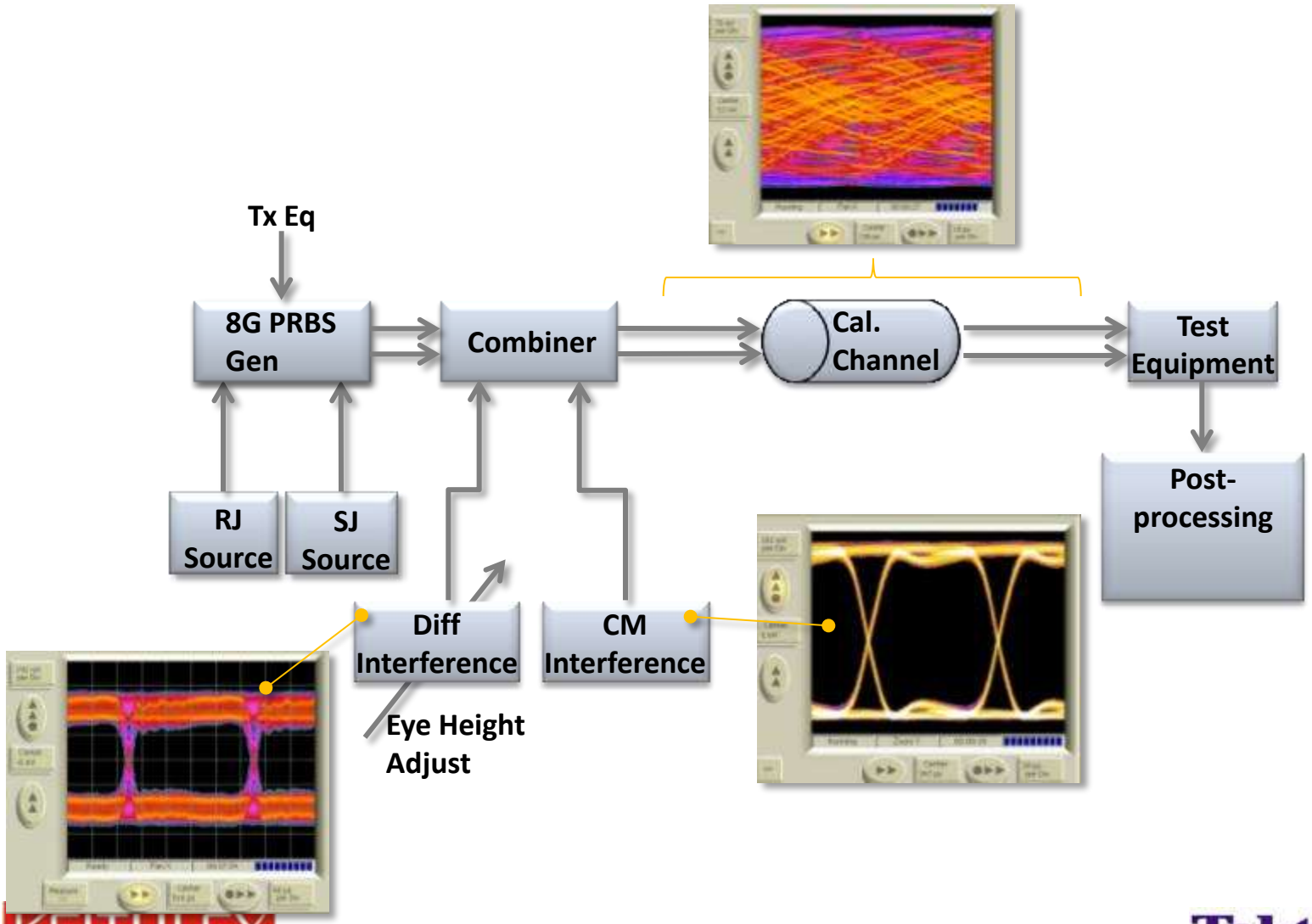

At the simplest level, receiver testing is composed of:

1. Send impaired signal to the receiver under test
2. The receiver decides whether the incoming bits are a one or a zero
3. The chip loops back the bit stream to the transmitter
4. The transmitter sends out exactly the bits it received
5. An error counter compares the bits to the expected signal and looks for mistakes (errors)

KEITHLEY
A Tektronix Company

Tektronix

# Stress Composition




KEITHLEY
A Tektronix Company

Tektronix®

# Components of a PCIe3 Receiver Test Solution

- BERTScope C Model
  - PG, stressed eye sources, ED
- New! DPP125C Option ECM
  - Eye opener, Clock doubler/Multiplier
- New! BSAITS125
  - CM/DM interference
  - ISI for Gen2 & Gen3
  - Option EXP for variable ISI
- New! CR125A Opt PCIE8G
  - PLL analysis for Gen1/2/3
- New! BSAPCI3 SW
  - Auto calibration, Link training, and test
- Cables, adapters, compliance boards
- DSA/DPO/MSO70K Series Oscilloscope
  - Stressed Eye Calibration

KEITHLEY
A Tektronix Company

Tektronix

# DPP125C with Option ECM

- Integrated reference clock multiplication to PCIe compliant 2.5 GHz, 5 GHz, and 8 GHz.
- Integrated eye opener functionality for testing DUTs with long channels.
- New microcontroller to provide more processing power.
- RS-232 interface enhancement to speed-up PCIe receiver equalization link training.
- SW to accommodate channel de-embedding and ISI fine adjustments.

KEITHLEY
A Tektronix Company

Tektronix®

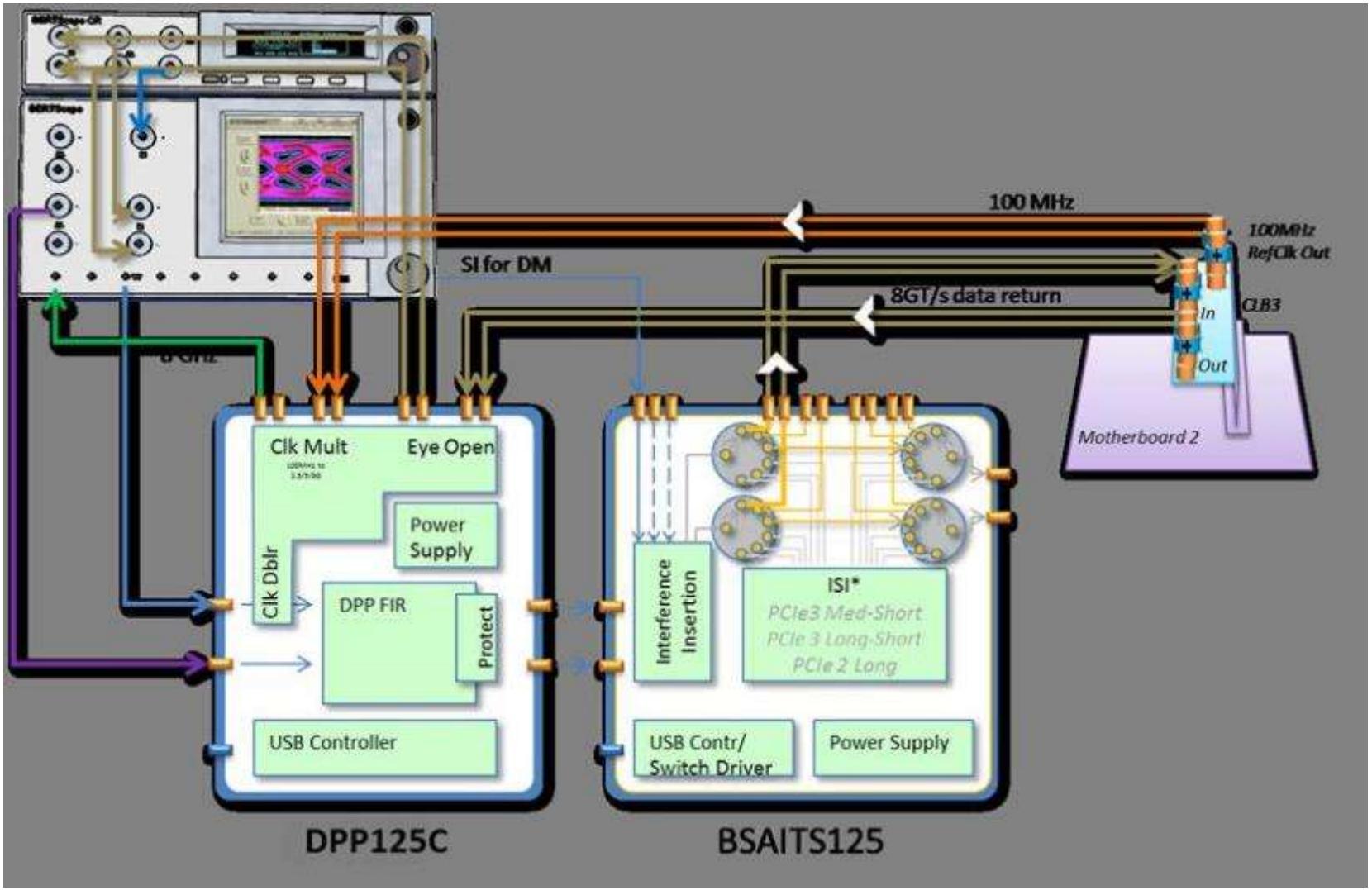
# BSAITS125 Interference Test Set

- Programmable, variable ISI for automated testing and precision setting
- Built-in compliant PCIe2 and PCIe3 Medium and Long ISI channels
- Integrated PCIe3 CM and DM interference combiner
- Integrated PCIe3 Base Spec CM interference calibration
- Continuously Variable, Expanded ISI for automated testing of multiple standards with Option EXP

KEITHLEY
A Tektronix Company

Tektronix®

# Typical PCIe3 Rx Test Configuration

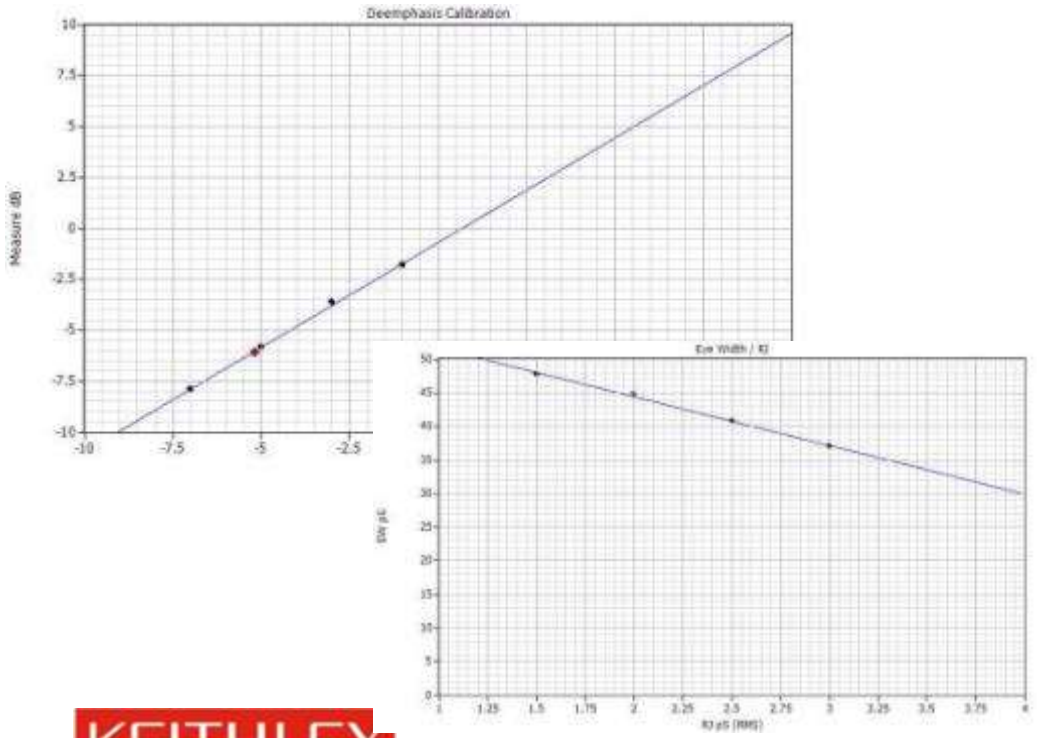


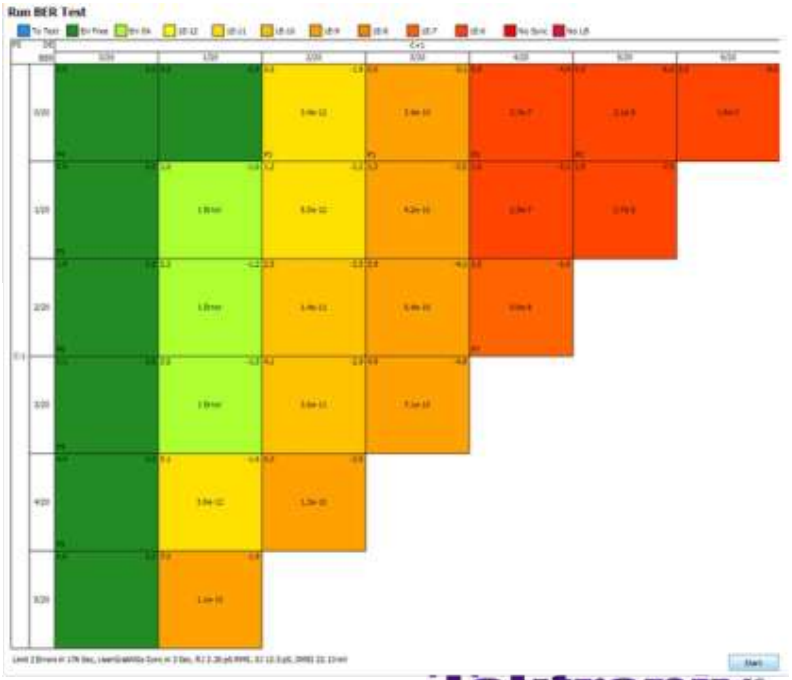

KEITHLEY
A Tektronix Company

Tektronix®

# BSAPCI3 PCIe 3.0 Automation SW

- Automated calibration, link training, loopback initiation, and testing.
- BER Map feature for TxEQ optimization.
- Reduces the time and minimizes the skill-set required to perform the calibration and testing.
- Increases the reliability and accuracy by removing inconsistencies with manual calibration.



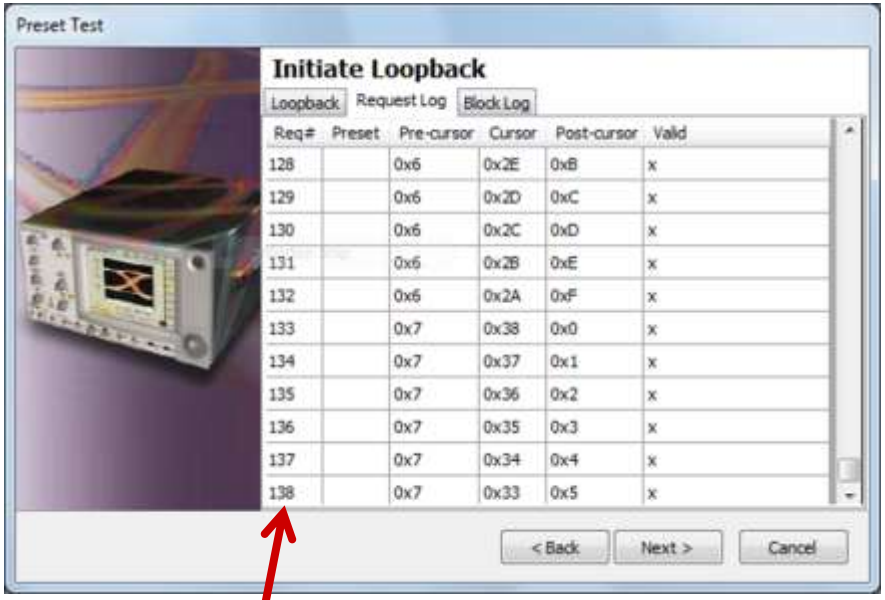



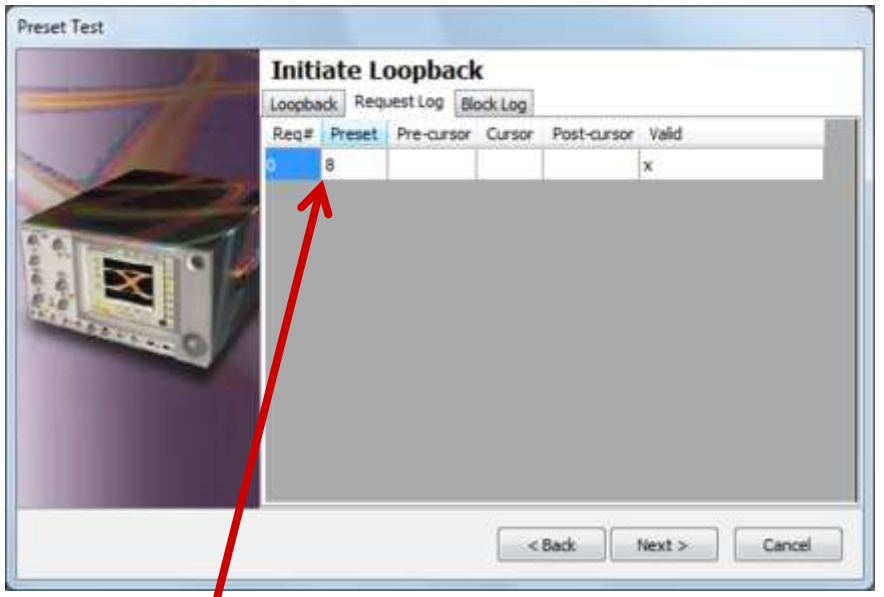

KEITHLEY
A Tektronix Company

Tektronix®

# Automated Link Equalization

- Loopback results: automation software provides complete equalization request log




- DUT 1 makes many equalization setting requests
- DUT 2 requests only one equalization preset

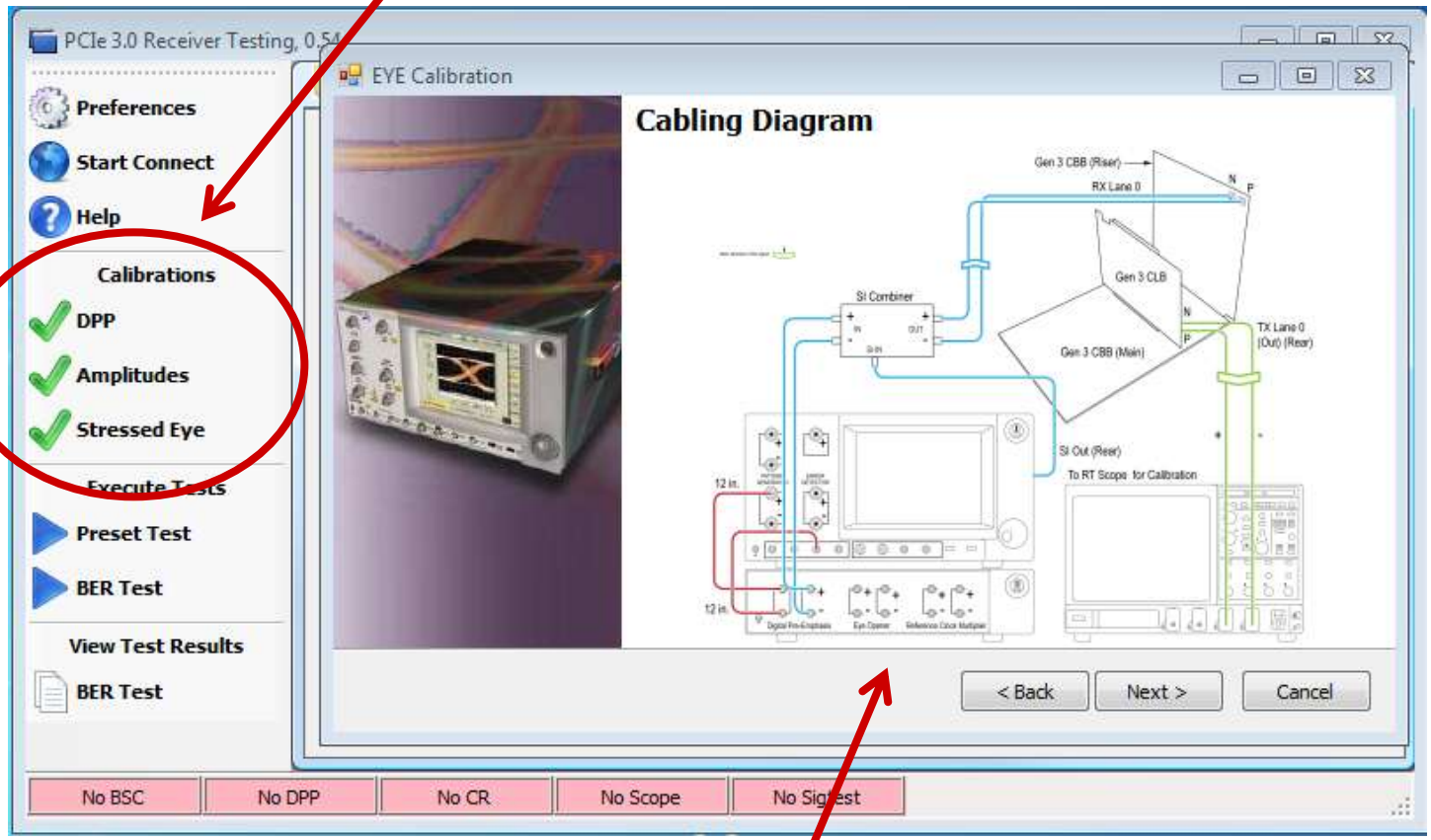
Tektronix

# Automatic Calibration

- Due to complex test setup and variations in DUTs and test equipment just dialing up the settings on the signal source is not sufficient
- Stress must be measured and adjusted
- Automatic calibration is used to achieve the right amount of stress
- Margin testing complements the compliance testing
  - Help understand your device's margins.
  - How much additional stress does it tolerate?

# Stressed Eye Calibration Setup

- Three required calibrations are fully automated

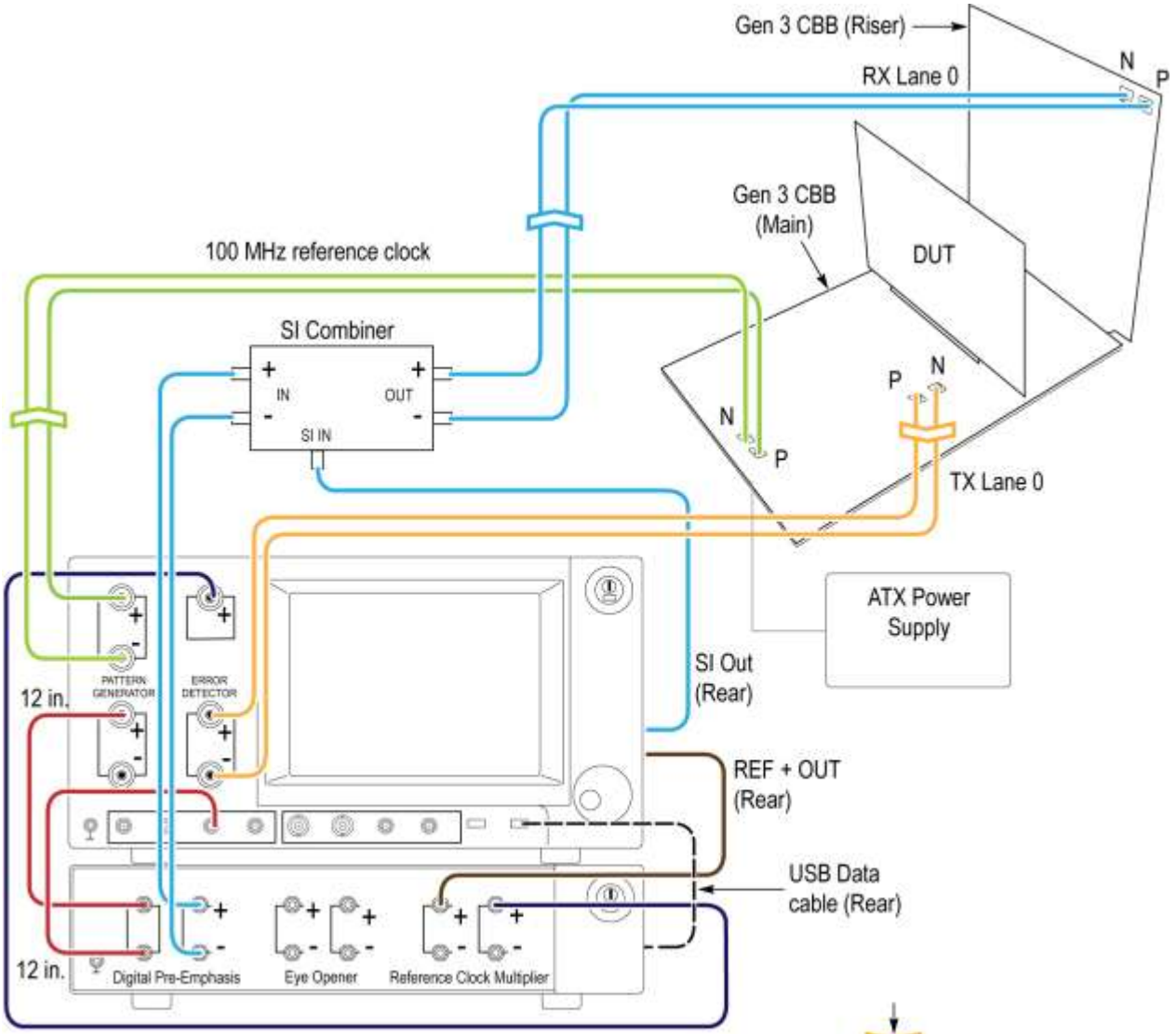



- Detailed cabling diagrams are provided for each calib

KEITHLEY
A Tektronix Company

Tektronix®

# Add-In Card: Receiver Stressed Eye Testing

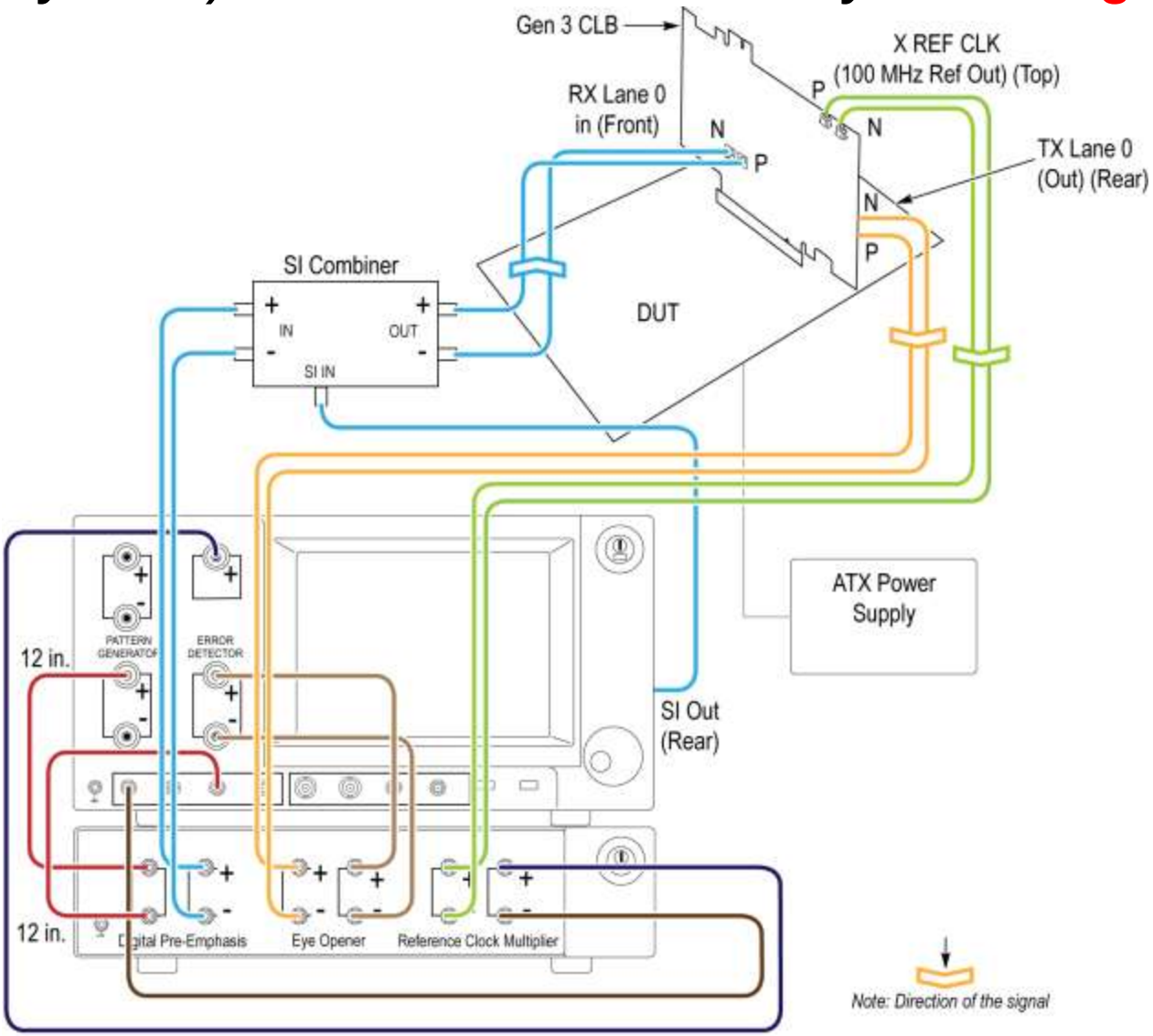



Add-In Card Connection Diagram: Receiver Stressed Eye Testing

KEITHLEY
A Tektronix Company

Tektronix

# Host (System): Receiver Stressed Eye Testing




Equipment (Host) Connection Diagram: Receiver Stressed Eye Testing

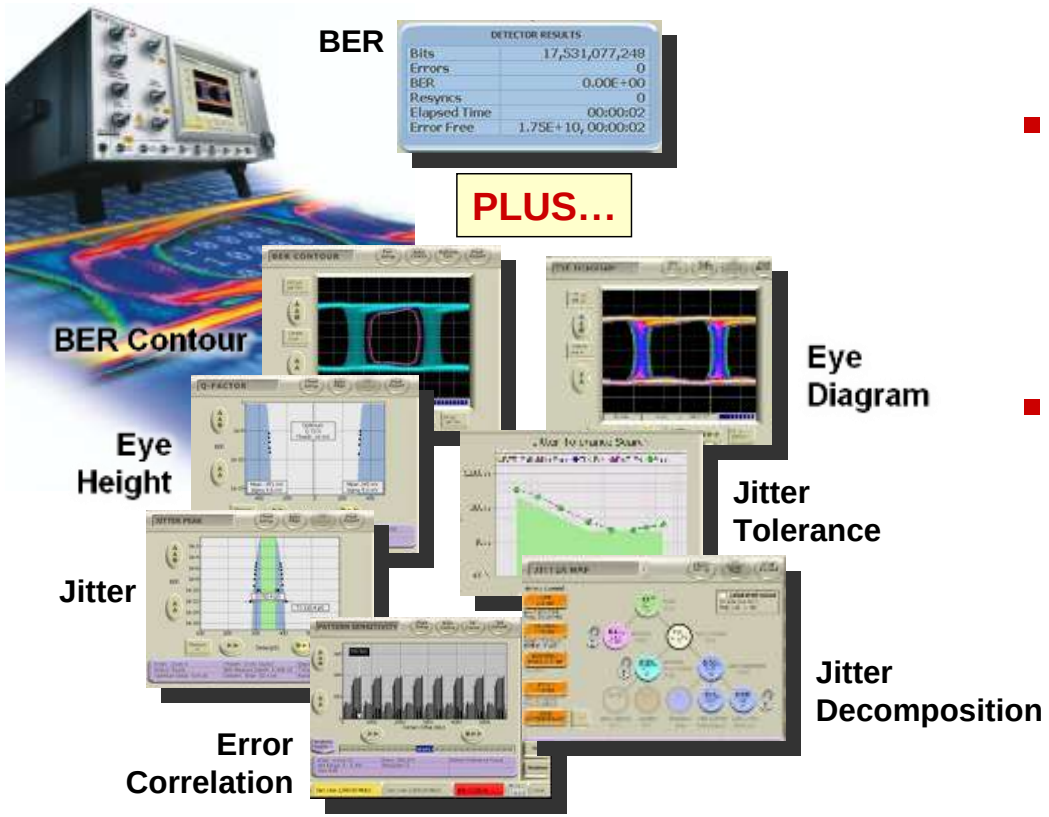
KEITHLEY
A Tektronix Company
Tektronix

# Rx Testing Summary

- Certainly the most complex type of testing
  - Due to complexity of equipment and procedures
- Extensive correlation studies in PCI-SIG have helped to streamline solutions
  - Similar stress signals
  - Guided calibration and test execution
  - Good correlation on the latest workshop
- Link Equalization detail and BER test matrix go beyond compliance testing and give visibility into DUT behavior and margins
- Successful Rx compliance and margin test gives you the confidence that the device passes when you get to the workshop

# Beyond Compliance: BERTScope Analysis Tools

- Besides being a BERT, the BERTScope's **"Scope" functionality** brings benefits that complement those of the Tektronix scopes
- Analysis tools are full featured and easy to use




- Frees up the scope for other tasks
- **Eye diagram for quick diagnosis** of synchronization and BER failure issues
- **Debug** challenging **signal integrity problems**
  - Error Location Analysis
  - Pattern Capture
  - Jitter Map
  - BER Contour

KEITHLEY
A Tektronix Company

Tektronix®

# PCIe Gen3 Protocol

KEITHLEY
A Tektronix Company

Tektronix®

# PCI Express Protocol Test Solution

## Software

- Module setup & trigger
- PCIe decoders
- Data windows:
  - Summary Profile
  - Transaction with BEV Flow control
  - Listing
  - Waveform

## Modules

- 8, 5, 2.5 GTs
- x8 & x4
- 8 State Triggering
- 8 GB memory
  - 16 GB for x16
- OpenEYE
- FastSYNC

## Probes

- x8 & x4 midbus
- x16, x8, x4, x1 slot interposers with Lane Converters
- Solder-down probe
- Gen2 probes for x8 & x4 midbus footprints rated to 5 GTs
- All probes rated to 8 GTs
- 6’ probe cables
- ScopePHY

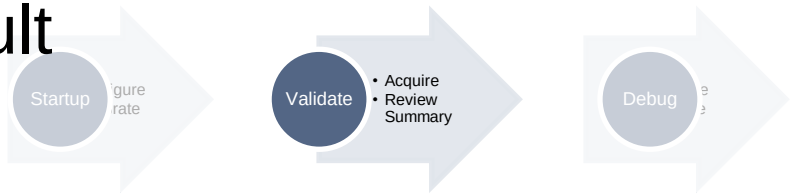
KEITHLEY
A Tektronix Company

## Mainframes

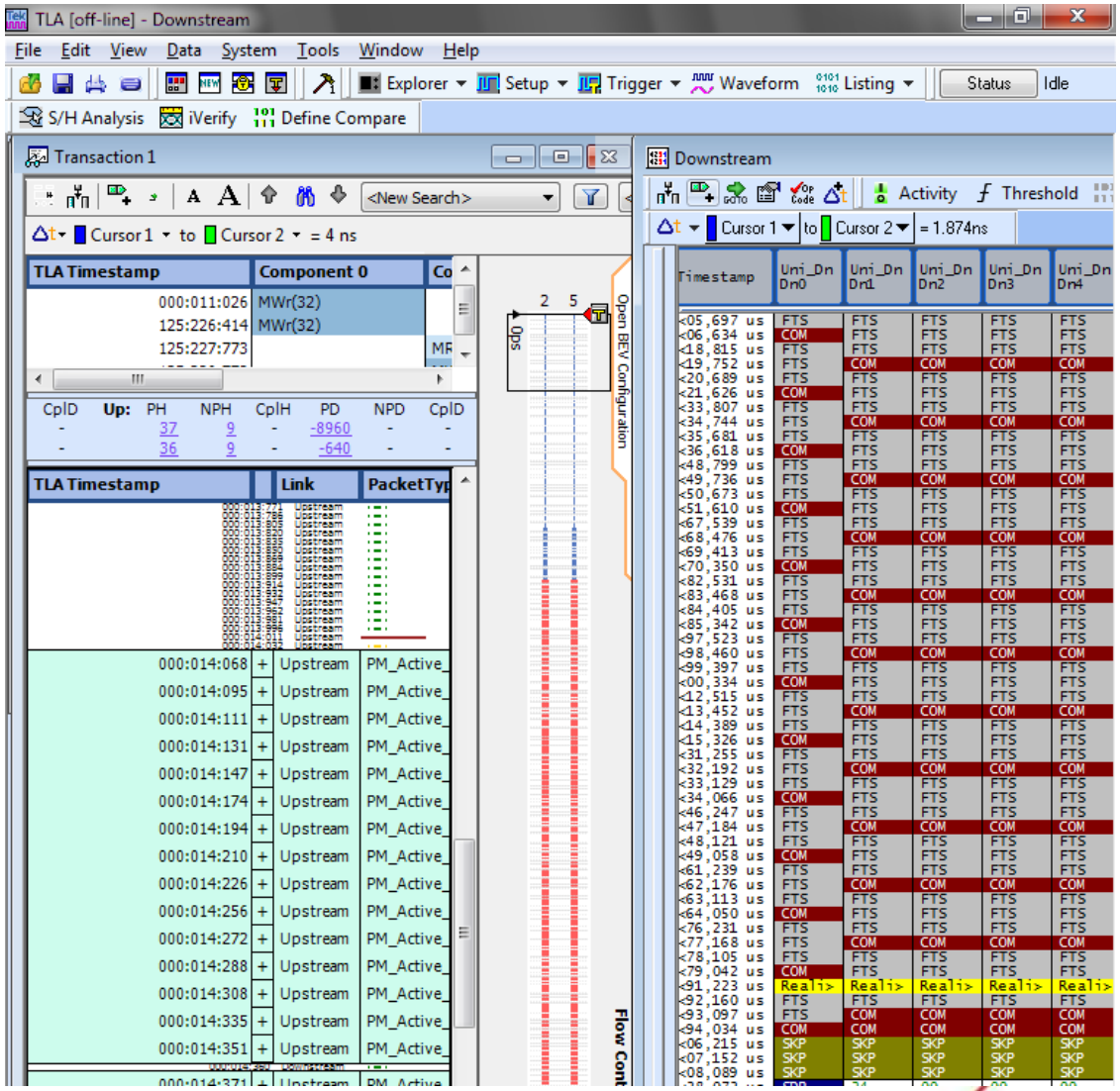
- 2 module portable mainframe with integrated 15” display & PC controller
- 6 module benchtop with GbE controller (requires PC)
- Single GUI & frame for system level debug of multi-buses

Tektronix®

# PCI Express Protocol Test Result




- Automatic display of Transaction Window with Listing Window
- Errors with timestamps and link direction
- Expanded Training sets with all of the TS data
- Default columns in Listing window




KEITHLEY
A Tektronix Company

# Gen4 Update

- Key attributes/requirements of PCIe 4.0
  - 16 GT/s, using scrambling, same as 8 GT/s, no encoding change
  - Maintains compatibility w/ PCIe installed base
  - Connector enhanced electrically (no mechanical changes)
  - Limited channel: ~12”, 1 connector; repeater for longer reach
- Uniform measurement methodology applied across all data rates
- New ‘SRIS’ independent RefClk modes
  - SRIS – Separate RefClk Independent SSC Architecture
- Rev 0.3 Base spec just introduced in PCI-SIG (June 2013)
  - Rev 0.9 no earlier than 1H/2015
  - Rev 1.0 no earlier than 2H/2015

# Gen4 Update

Latest Gen4 Update @ PCIe DevCon on Tue/Wed, June 25-26

- Tx Jitter – Analysis solution available today with PCE3.
- Tx EQ – CEM and Embedded will have limited change. Base might require Sampling solution.
- Rx – Similar approach at 16Gb/s.

## Transmitter Jitter Spec

- PCIe 4.0 uses same jitter parameters as PCIe 3.0
  - ✓ $T_{TX-UPW-TJ}$, $T_{TX-UPW-DJDD}$, $T_{TX-DDJ}$, $T_{TX-UTJ}$ and $T_{TX-UDJDD}$
  - ✓ Jitter will need to scale approximately with bitrate
  - ✓ De-embedding approach will likely remain the same
- PCIe 1.x and PCIe 2.x jitter parameters will be recast into the same form as the PCIe 3.0 parameters
  - ✓ Backward compatibility will be guaranteed
  - ✓ Some PCIe 1.x/2.x parameters will be effectively tightened
  - ✓ Example: PCIe 2.x $T_{MIN-PULSE}$ parameter will be converted into $T_{TX-UPW-TJ}$ and $T_{TX-UPW-DJDD}$


Copyright © 2012, PCI-SIG, All Rights Reserved


## PCIe 4.0 Rx Specification

- Will continue to rely upon a stressed eye approach where both EH and EW are stressed
  - ✓ Calibration channels IL will need to be reduced to yield ~24 dB at 8 GHz
  - ✓ Behavioral package model needs to comprehend reduced $C_{PAD}$ or include T-coil models
  - ✓ Behavioral DFE model to have increased number of taps, at least 2
  - ✓ More capable CTLE model


Copyright © 2012, PCI-SIG, All Rights Reserved

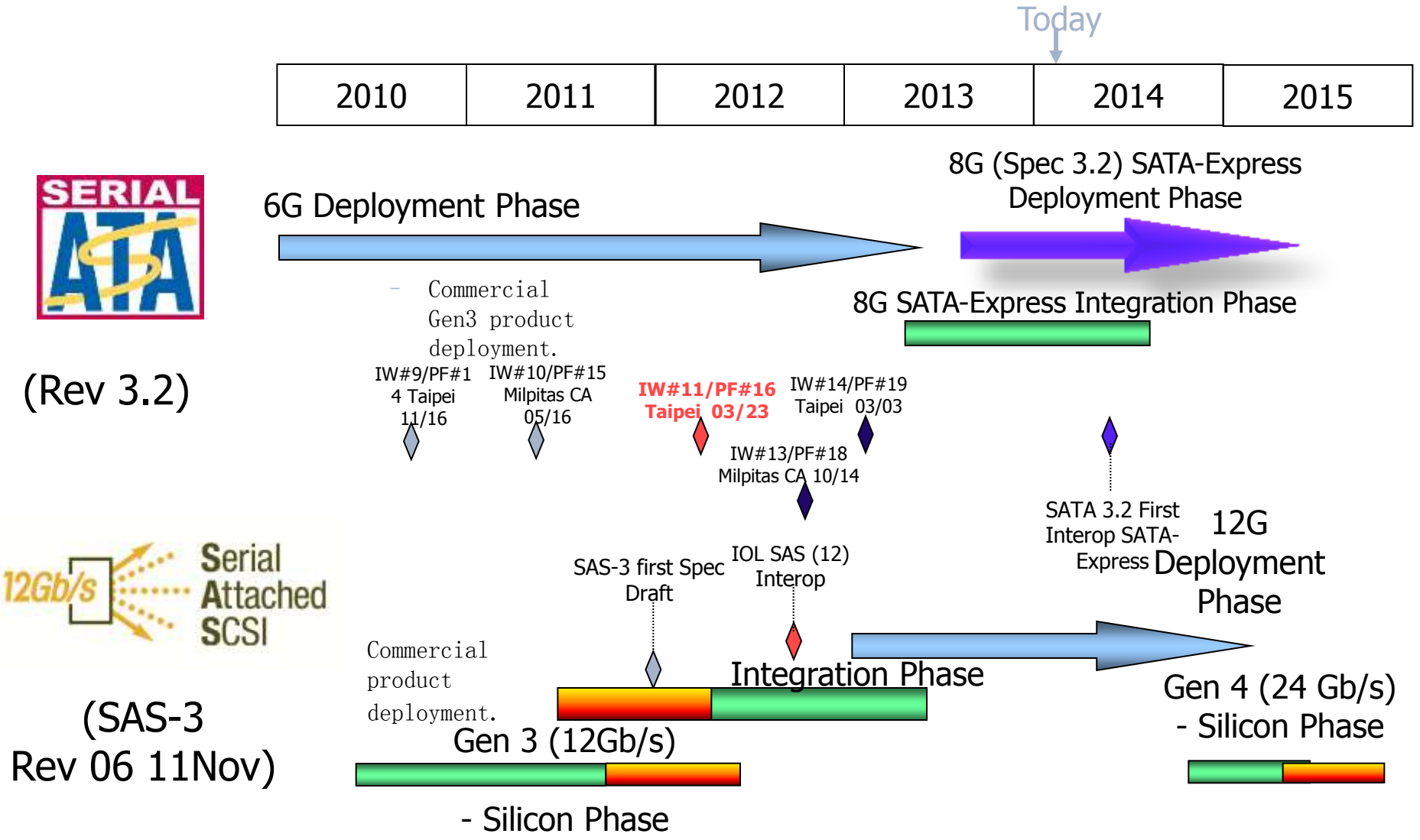

## Transmitter Equalization

- Max PCIe 4.0 channel IL remains approx the same s for PCIe 3.0
- Plan is to retain same equalization presets
  - ✓ Training will require that only a subset of the presets be used (P7 and P8)
- Equalization coefficient range and resolution also are intended to remain unchanged
- EIEOS signaling will likely change such that no TxEQ is applied during the EIEOS interval


Copyright © 2012, PCI-SIG, All Rights Reserved


KEITHLEY
A Tektronix Company
Tektronix®

# SATA and SAS Industry Timeline




KEITHLEY
A Tektronix Company

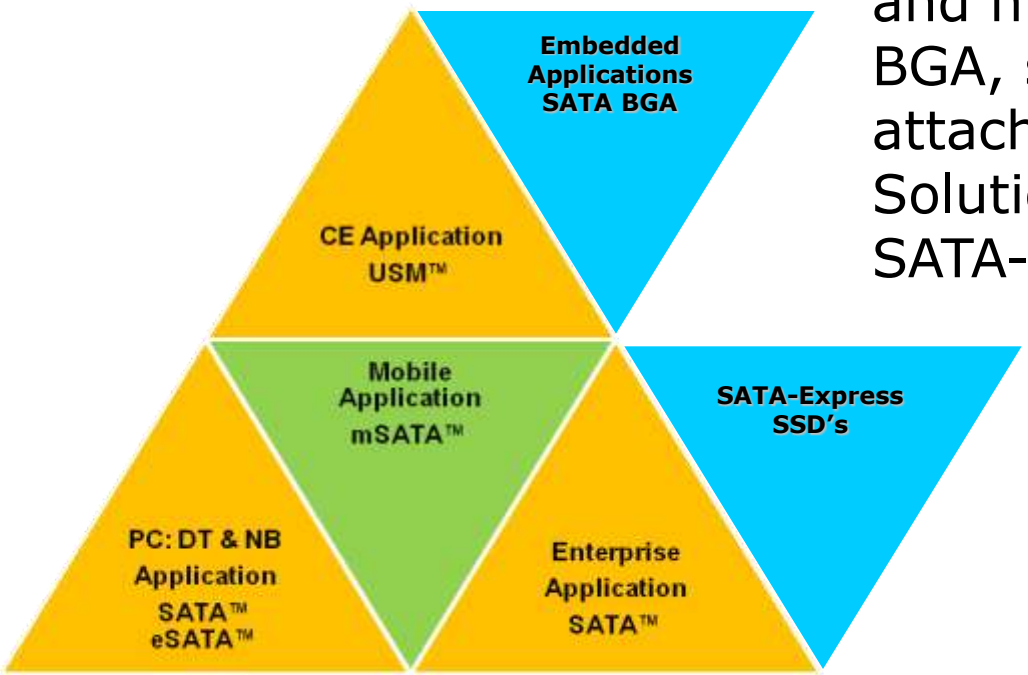
Tektronix

# SATA3 Tx & Rx Solution

KEITHLEY
A Tektronix Company

Tektronix®

# The SATA Ecosystem: Now




Today, SATA is expanding in specialized low power, compact and high performance areas with BGA, small form factor, direct attach (M.2) and SATA-Express Solutions recently approved by SATA-IO.

# NEW SATA 3.2 Specification

- **SATA Express:**
  - Includes both SATA and PCIe signaling
  - Hosts supports both SATA or PCIe storage device.
  - With PCIe transfer rates of up to 2 GB/s (2 lanes of PCIe 3.0), compared with today's SATA technology at 0.6 GB/s.
- **M.2:**
  - SATA revision 3.2 also incorporates the M.2 form factor, enabling small form-factor M.2 SATA SSDs suitable for thin devices such as tablets and notebooks.
- Additional features of the SATA-IO Revision 3.2 Specification include:
  - microSSD–standard for embedded solid state drives (SSDs) that enables developers to produce single-chip SATA implementations for embedded storage applications.
  - Universal Storage Module (USM)– enables removable and expandable storage for consumer electronic devices. SATA revision 3.2 introduces USM Slim, which reduces module thickness, allowing smaller removable storage solutions.
  - DevSleep– the lowest level of power management yet, where the drive is almost completely shut down, meeting the requirements of new always on, always connected mobile devices such as Ultrabooks™.

# What's new with SATA testing?

- **UHost:** A SATA host that provides for attachment of a Gen1i/Gen2i/Gen3i endpoint device directly to the mating connection of the Uhost… (i.e. a "no cable" solution)
- **TSG-04**
  - Incorporate ECN066 which affects the Pass/Fail criteria
  - Vcm,acTX measured at a maximum of 50 mVp-p ( Gen2i, Gen2m), 100 mVp-p (Gen1u, Gen2u, Gen3u) and 120 mVp-p (Gen3i).
- **TSG-13**
  - The Total Jitter is measured with LBP. Measurements with all other patterns (HFTP, MFTP, and LFTP) are Informative.
- **TSG-15**
  - For a Gen3u UHost PUT, the Gen3i CIC channel is not used and the measurement is made directly into the lab load.
  - CIC included for Gen3u Uhost calibration but not included for testing

# SATA Transmitter Tests

| Tests | UTD 1.4.2 | UTD 1.4.3 | UTD 1.5 | |
|---|---|---|---|---|
| PHY-01 : Unit Interval | Normative | Normative | Normative | PHY |
| PHY-02 : Frequency Long Term Stability | Normative | Normative | Normative | |
| PHY-03 : Spread-Spectrum Modulation Frequency | Normative | Normative | Normative | |
| PHY-04 : Spread-Spectrum Modulation Deviation | Normative | Normative | Normative | |
| TSG-01 : Differential Output Voltage | Normative | Normative | Normative | TSG |
| TSG-02 : Rise/Fall Time | Normative | Informative | Informative | |
| TSG-03 : Differential Skew | Normative | Informative | Informative | |
| TSG-04 : AC Common Mode Voltage | Normative | Normative | Normative/Update | |
| TSG-05 : Rise/Fall Imbalance | Obsolete | Obsolete | Obsolete | |
| TSG-06 : Amplitude Imbalance | Obsolete | Obsolete | Obsolete | |
| TSG-07 : Gen1 (1.5 Gbps) TJ at Connector, Clock to Data, fBAUD/10 | Obsolete | Obsolete | Obsolete | |
| TSG-08 : Gen1 (1.5 Gbps) DJ at Connector, Clock to Data, fBAUD/10 | Obsolete | Obsolete | Obsolete | |
| TSG-09 : Gen1 (1.5 Gbps) TJ at Connector, Clock to Data, fBAUD/500 | Normative | Normative | Normative | |
| TSG-10 : Gen1 (1.5 Gbps) DJ at Connector, Clock to Data, fBAUD/500 | Normative | Normative | Normative | |
| TSG-11 : Gen2 (3 Gbps) TJ at Connector, Clock to Data, fBAUD/500 | Normative | Normative | Normative | |
| TSG-12 : Gen2 (3 Gbps) DJ at Connector, Clock to Data, fBAUD/500 | Normative | Normative | Normative | |
| TSG-13 : Gen3 (6 Gbps) Transmit Jitter | Normative | Normative | Normative/Update | |
| TSG-14 : Gen3 (6 Gbps)TX Maximum Differential Voltage Amplitude | Normative | Normative | Normative | |
| TSG-15 : Gen3 (6 Gbps) TX Minimum Differential Voltage Amplitude | Normative | Normative | Normative/Update | |
| TSG-16 : Gen3 (6 Gbps) Tx AC Common Mode Voltage | Normative | Normative | Obsolete | |
| OOB-01 : OOB Signal Detection Threshold | Normative | Normative | Normative | OOB |
| OOB-02 : UI During OOB Signaling | Normative | Normative | Normative | |
| OOB-03 : COMINIT/RESET and COMWAKE Transmit Burst Length | Normative | Normative | Normative | |
| OOB-04 : COMINIT/RESET Transmit Gap Length | Normative | Normative | Normative | |
| OOB-05 : COMWAKE Transmit Gap Length | Normative | Normative | Normative | |
| OOB-06 : COMWAKE Gap Detection Windows | Normative | Normative | Normative | |
| OOB-07 : COMINIT/COMRESET Gap Detection Windows | Normative | Normative | Normative | |

# Transmitter Test Patterns

- **HFTP (High Frequency Test Pattern)**

  0101010101 0101010101

  D10.2 D10.2

- **MFTP (Mid Frequency Test Pattern)**

  0011001100 1100110011

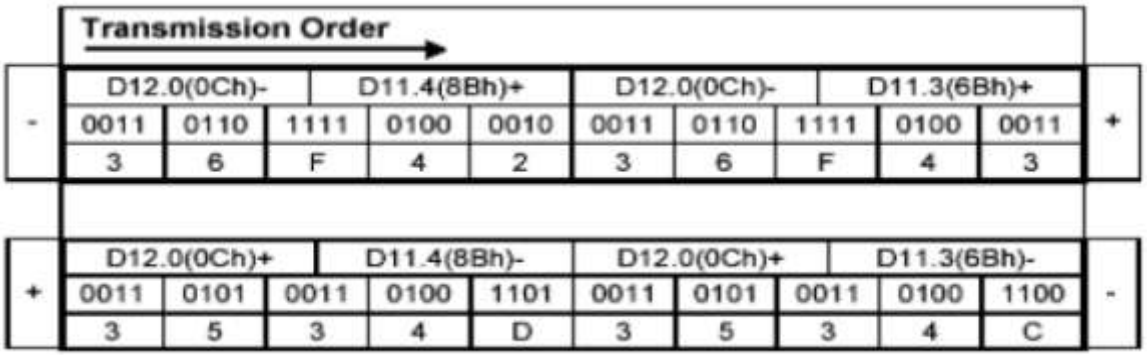
  D24.3 D24.3

- **LFTP (Low Frequency Test Pattern)**

  0111100011 1000011100

  D30.3 D30.3

- **LBP (Lone Bit Pattern)**

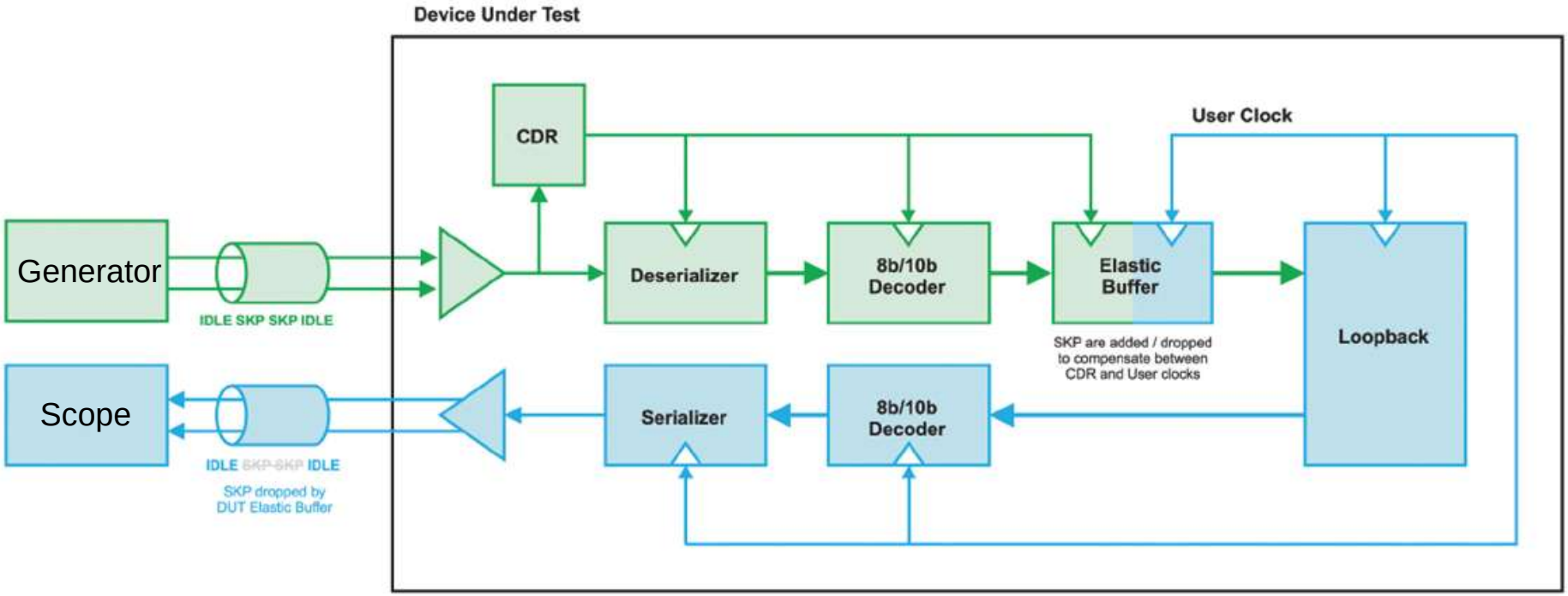



KEITH
A Tektronix Company

Tektronix

# Test Pattern Generation

- BIST-TSA: Self generated transmission of pattern (required)
  - T: Transmit only (no Rx required)
  - S: Scramble Bypass
  - A: ALIGN Bypass
- BIST-L: Far End Retimed Loopback (required)
  - Signal generator sends in pattern DUT retransmit same pattern



# AWG Device State Control

| | |
|---|---|
| Real Time Scope | DPO72004B ( GPIB8::1::INSTR ) |
| BIST-L initialization by | **Auto** |
| Set scope scale, resolution and sampling rate | Custom Utility<br>Operation without AWG<br>User Defined Batch Script |
| Set vertical scales automatically | |
| BIST-L validation required | Always |
| Number of times AWG is turned ON/OFF for putting DUT in BISTL mode | 2 |
| Horizontal scale for PHY-TSG BIST-L acquisition (us/div) | 4 |
| Resolution for PHY-TSG BIST-L acquisition (ps/pt) | 20 |
| OOB validation required | First time only |

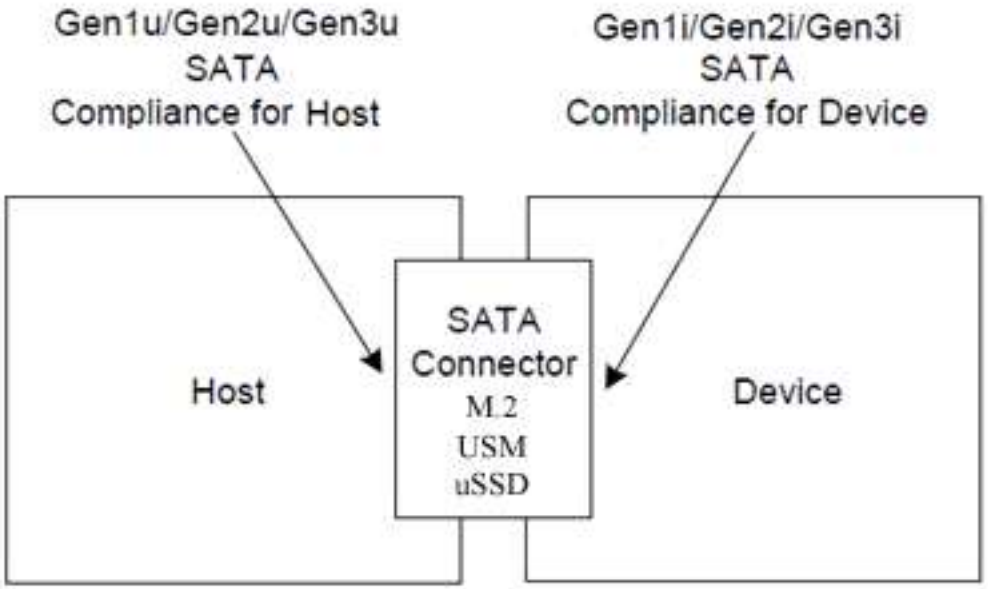
- DUT control a significant challenge
  - BIST-L (loopback) required for compliance
- AWG has a successful track record of DUT control
  - Initiates loopback while seamlessly transitioning to Tx/Rx testing
- 3rd party tools available (Drivemaster, serial port control)

KEITHLEY
A Tektronix Company

Tektronix®

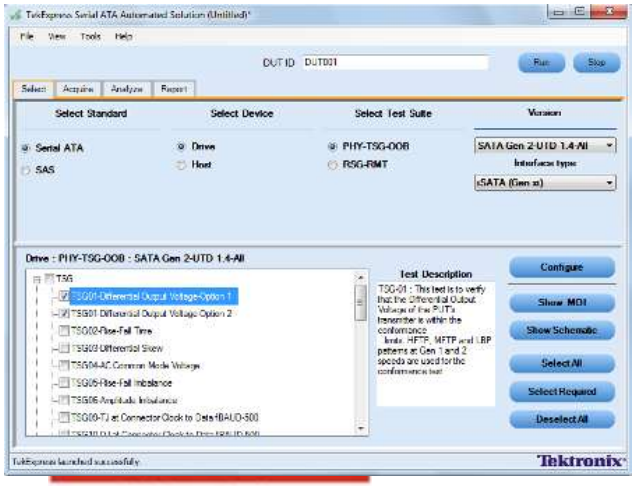
# ‘Direct Attach’ Usage Models

- Formally referenced as M.2, USM, or MicroSSD
- Devices meet Gen1i/2i/3i specifications
- Hosts meet Gen1u/2u/3u specifications



# SATA PHY Test Solution

- TekExpress SATA-TSG software
  - NEW TekExpress version in Q2 (M.2, mSATA, etc.)
- AWG BIST-L library
  - Updated periodically, for latest chipset contact Randy White
- SATA 6 Gb/s serial error detector (scope/BSA symbol filtering)
  - Scope/AWG provides single setup for Tx and Rx
  - BERTScope roadmap includes Idle state and sequencing

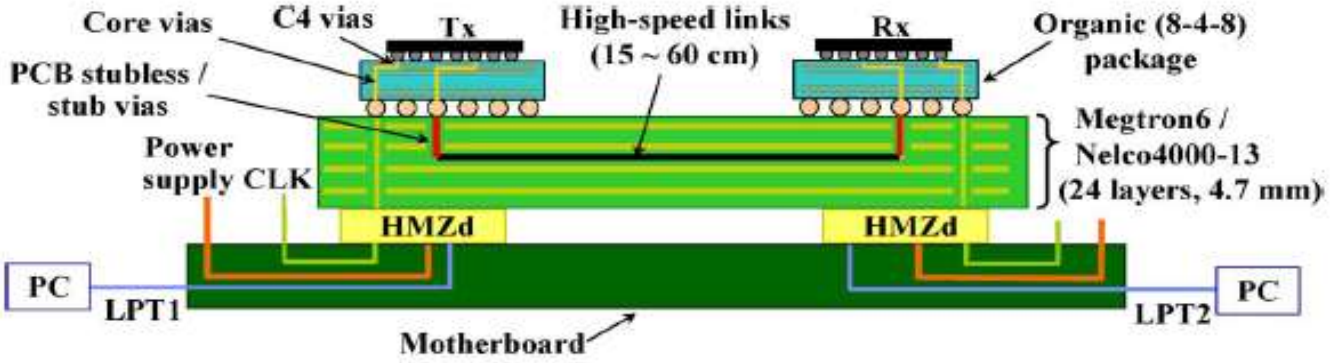


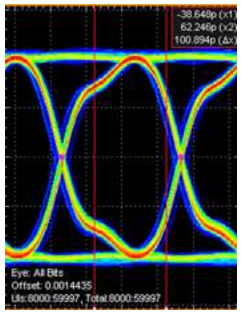
A Tektronix Company

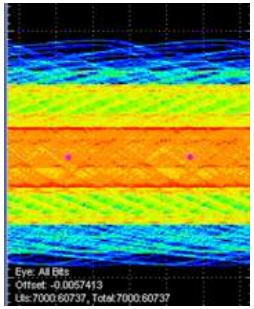
# SAS3 -- Challenge to 12Gbps

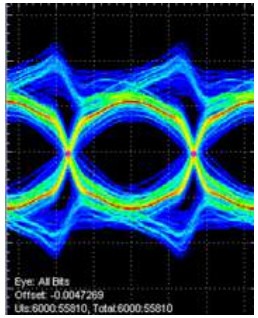
# 12G+ Design Problem:
## 1000mV, FFE, Crosstalk, DFE, 50mV

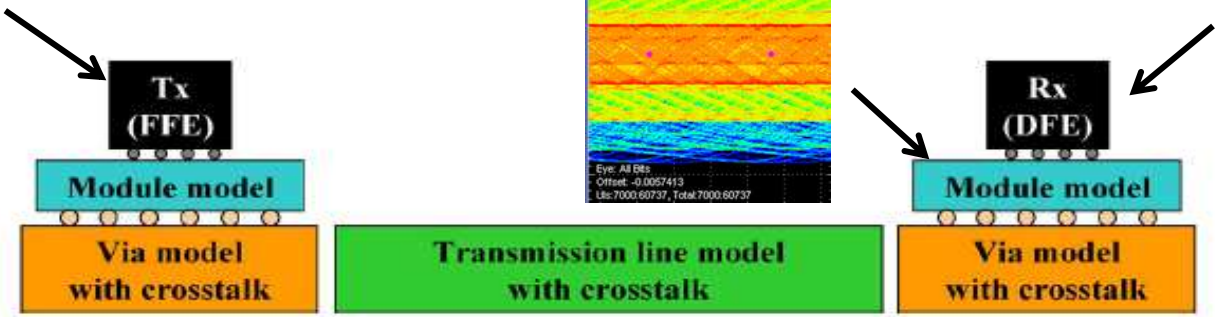
- Crosstalk and signal loss problems are the largest design challenge today.
- Significant advances in high tap count Decision Feedback Equalization are key to operating at 12G+.







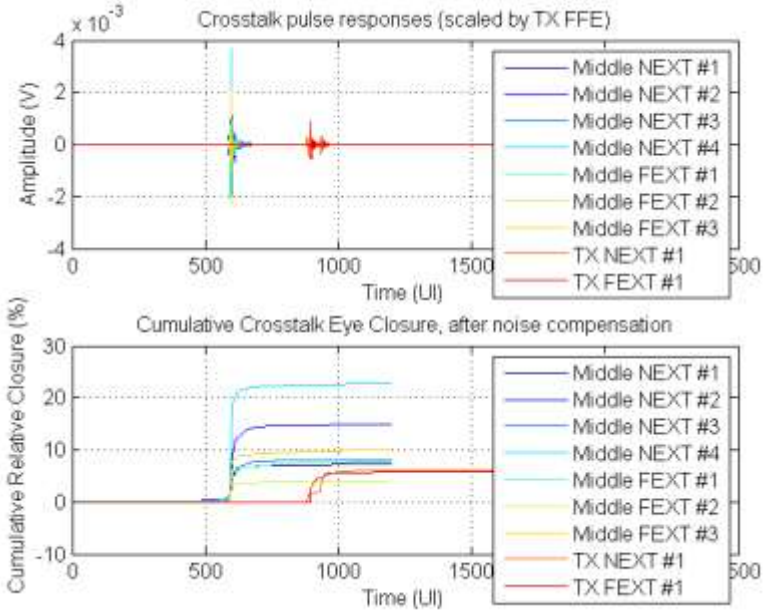



KEITHLEY
A Tektronix Company

Tektronix®

# Measurement for Crosstalk/ISI Evaluation

- SAS3_EYEOPENING* Measurement for accurate analysis of ISI and crosstalk effects
- Provides measure of relative vertical eye opening after reference equalization



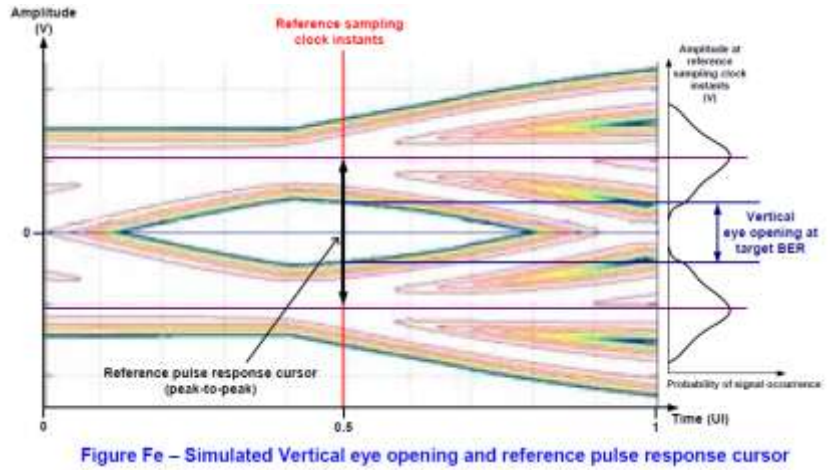




Figure Fe – Simulated Vertical eye opening and reference pulse response cursor

*Source:* 12-244r3

*Note, this measurement is similar to the SAS-2 Waveform Distortion Penalty (WDP) measurement but also includes Tx EQ in addition to Rx DFE. The code was provided and distributed through the T10 Technical Committee and permission has been granted for Tektronix to reuse.

KEITHLEY
A Tektronix Company

Tektronix®

# SAS3_EYEOPENING provides 4 different metrics

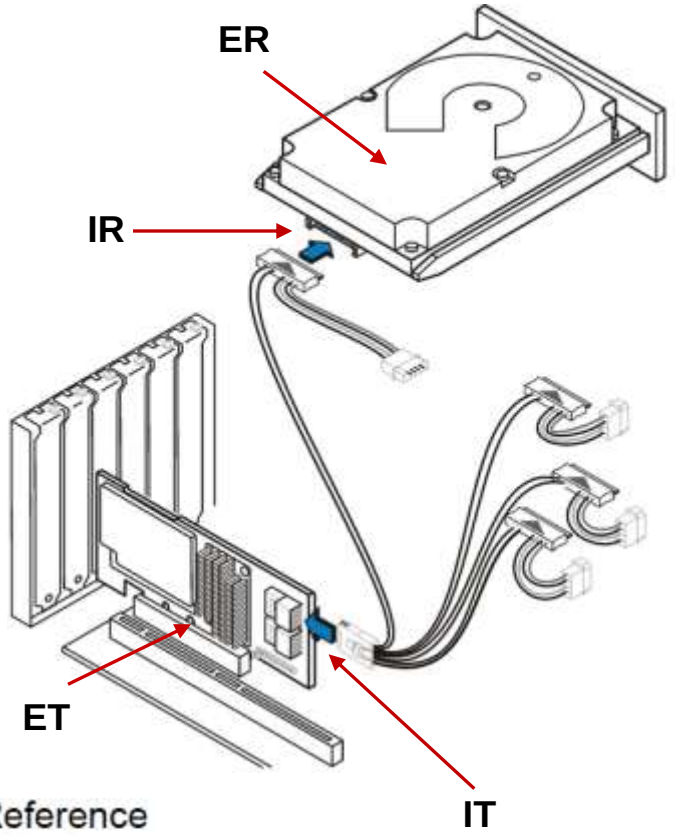
1. Relative Vertical Eye Opening: A direct indication of how much margin there is after equalization
   - Takes into account un-compensable ISI and crosstalk
   - ISI and crosstalk broken down in report
2. Main Cursor Amplitude: A direct indication of the amplitude after equalization
   - Assumes 800 mVppd max. TX launch amplitude, unless data is captured
3. Maximal FFE correction: A direct indication of how much FFE correction is required by the transmitter
   - Max(abs(Cpre/Ccntr,Cpost/Ccntr))
4. - Maximal DFE correction: A direct indication of how much DFE correction is required by the receiver
   - Max(abs(DFE/Main))

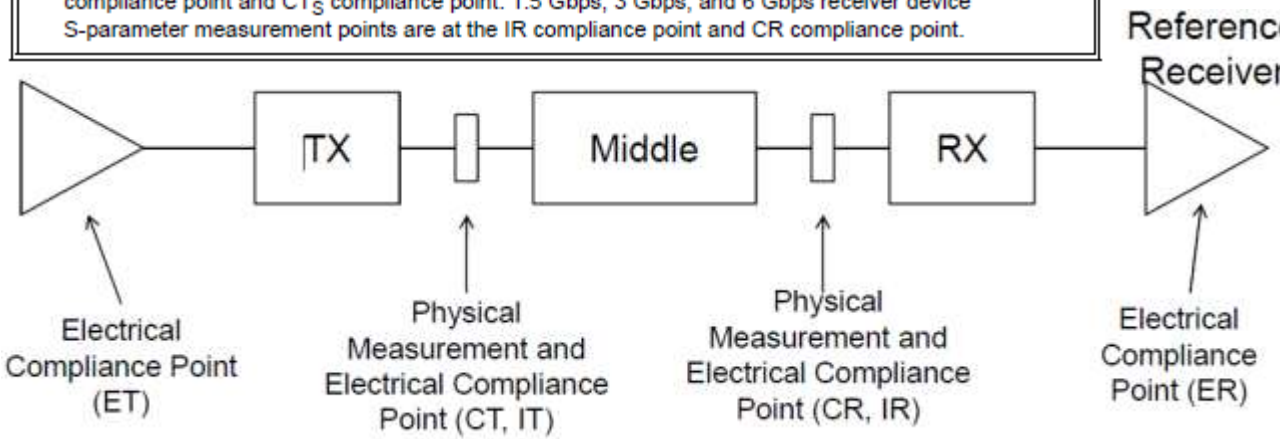
# A Note about SAS Test Points

Table 3 — 1.5 Gbps, 3 Gbps, and 6 Gbps compliance points

| Compliance point | Type | Description |
|---|---|---|
| IT | intra-enclosure (i.e., internal) | The signal from a transmitter device (see 3.1.110), as measured at probe points in a test load attached with an internal connector. |
| $IT_S$ [a] | intra-enclosure (i.e., internal) | The location of a transmitter device where S-parameters are measured and where the TxRx connection begins. This location is at the transmitter device side of the internal connector with a test load or a TxRx connection attached with an internal connector. |
| IR | intra-enclosure (i.e., internal) | The signal going to a receiver device (see 3.1.77), as measured at probe points in a test load attached with an internal connector. |
| CT | inter-enclosure (i.e., cabinet) | The signal from a transmitter device, as measured at probe points in a test load attached with an external connector. |
| $CT_S$ [a] | inter-enclosure (i.e., cabinet) | The location of a transmitter device where S-parameters are measured and where the TxRx connection begins. This location is at the transmitter device side of the external connector with a test load or a TxRx connection attached with an external connector. |
| CR | inter-enclosure (i.e., cabinet) | The signal going to a receiver device, as measured at probe points in a test load attached with an external connector. |

[a] Because the trained 1.5 Gbps, 3 Gbps, and 6 Gbps transmitter device S-parameter specifications do not include the mated connector, transmitter device S-parameter measurement points are at the $IT_S$ compliance point and $CT_S$ compliance point. 1.5 Gbps, 3 Gbps, and 6 Gbps receiver device S-parameter measurement points are at the IR compliance point and CR compliance point.



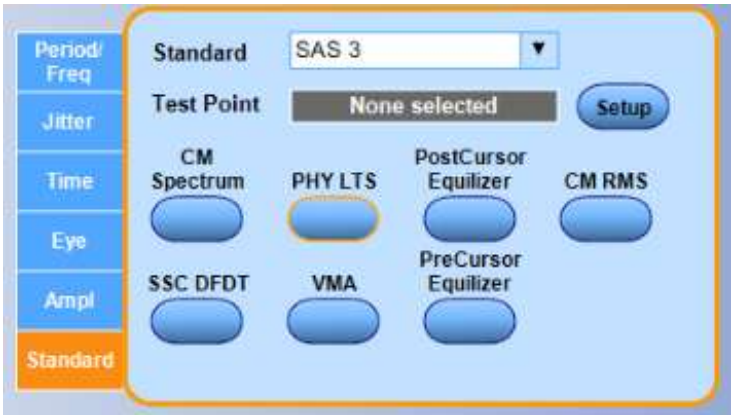



Tektronix®

# SAS-3 PHY Transmitter Solution

| | |
|---|---|
| **Group 1 – OOB Signaling** | |
| 5.1.1 | Maximum Noise During OOB Idle |
| 5.1.2 | OOB Burst Amplitude |
| 5.1.3 | OOB Offset Delta |
| 5.1.4 | OOB Common Mode Delta |
| **Group 2 – Spread Spectrum Clocking (SSC) Requirements** | |
| 5.2.1 | SSC Modulation Type |
| 5.2.2 | SSC Modulation Frequency |
| 5.2.3 | SSC Modulation Deviation |
| 5.2.4 | SSC Balance |
| 5.2.5 | SSC DFDT |
| **Group 3 – NRZ Data Signaling Requirements** | |
| 5.3.1 | Physical Link Rate Long Term Stability |
| 5.3.2 | Common Mode RMS Voltage Limit |
| 5.3.3 | Common Mode Spectrum |
| 5.3.4 | Peak to Peak Voltage |
| 5.3.5 | Voltage Modulation Amplitude (VMA) |
| 5.3.6 | Equalization |
| 5.3.7 | Rise Time |
| 5.3.8 | Fall Time |
| 5.3.9 | Random Jitter (RJ) |
| 5.3.10 | Total Jitter (TJ) |
| 5.3.11 | Waveform Distortion Penalty (WDP) |
| 5.3.12 | SAS3_EYEOPENING |
| 5.3.13 | Pre Cursor Equalization Ratio |
| 5.3.14 | Post Cursor Equalization Ratio |
| 5.3.15 | Transition Bit Voltage PK-PK (VHL) |
| 5.3.16 | Unit Interval |

SAS-3 1.5/3/6/12 Gb/s Tx Test Software




TekExpress SAS3-TSG Automation Software

# SAS-3 PHY Transmitter Solution

*Option SAS3-TSG*

- Automated transmitter validation for 1.5, 3, 6 and 12 Gb/s SAS physical layer specification
- Integrated SAS3_EYEOPENING and WDP* measurements for accurate analysis of ISI and crosstalk effects and relative vertical eye opening after reference equalization
- Easily reconfigure existing measurements to create user-specified test parameters or test limits
- Multiple plots and measurement configurations provides a quick comparison of the same acquired data with different settings
- Simultaneous two lane testing of primary and secondary ports
- Detailed test reports with screenshots, setup details, and pass/fail limits

* Requires Option SAS3-TSGW

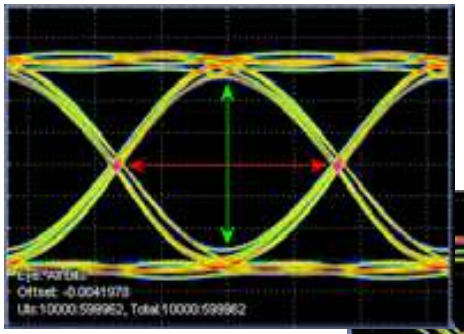
KEITHLEY
A Tektronix Company

Tektronix®

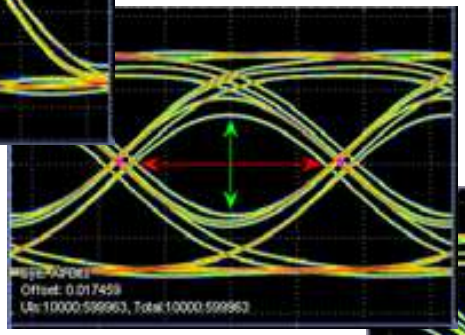
# Beyond Compliance

- How much margin is there in my design?
- How many DFE/FFE taps are needed to meet the system budget?
- What is longest channel (cable/backplane) the system can tolerate?
- How does process/voltage/temperature affect device performance?

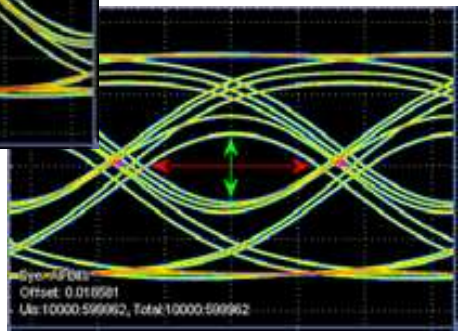
**1m cable**



**2m cable**



**3m cable**

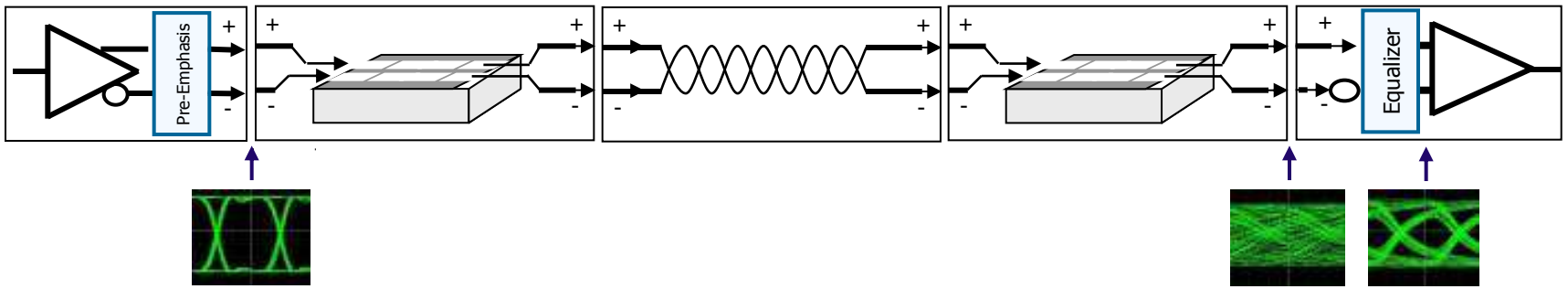


KEITHLEY
A Tektronix Company

Tektronix®

# Flexible Link Analysis Tools

- DFE/FFE modeling
  - Reference equalizer vs. vendor-specific (IBIS-AMI)
  - Equalization key differentiator for PHY vendors
- Enhanced de-embedding
  - Full four-port network characterization
- Channel emulation for margin analysis




KEITHLEY
A Tektronix Company

Tektronix

# Recommended Equipment

The following components are required for performing SAS12 Tx measurements

- DPO/MSO70000C/D/DX Series Oscilloscope with Opt. 2XL or higher
  - 12.5 GHz or higher recommended for 1.5, 3, or 6 Gb/s
  - 20 GHz or higher recommended for 12 Gb/s
- DPOJET Advanced (DJA) - Prerequisite
- Option SAS3-TSG & SAS3-TSGW (required for WDP measurements)
- Test Fixtures:
  - TF-SAS-TPA-R SAS Gen3 Receptacle Adapter (drive form factor) or
  - TF-SASHD-TPA-R miniSASHD 12G SAS Receptacle (mini SAS HD 4i/x cables) or
  - Set of TF-SASHD-TPAR-P miniSASHD 12G SAS (Right Side) Plug and TF-SASHD-TPAL-P miniSASHD 12G SAS (Left Side) Plug (x8)
- PMCABLE1M or equivalent Phase  Matched Cable Set (qty: 2)

# SAS 12 Gb/s Rx Test Setup

- Similar to SAS 6 Gb/s Rx configuration
- Rx calibration -> CJTPAT -> BER test
- Tektronix Method of Implementation (MOI) provides complete Rx Test procedure

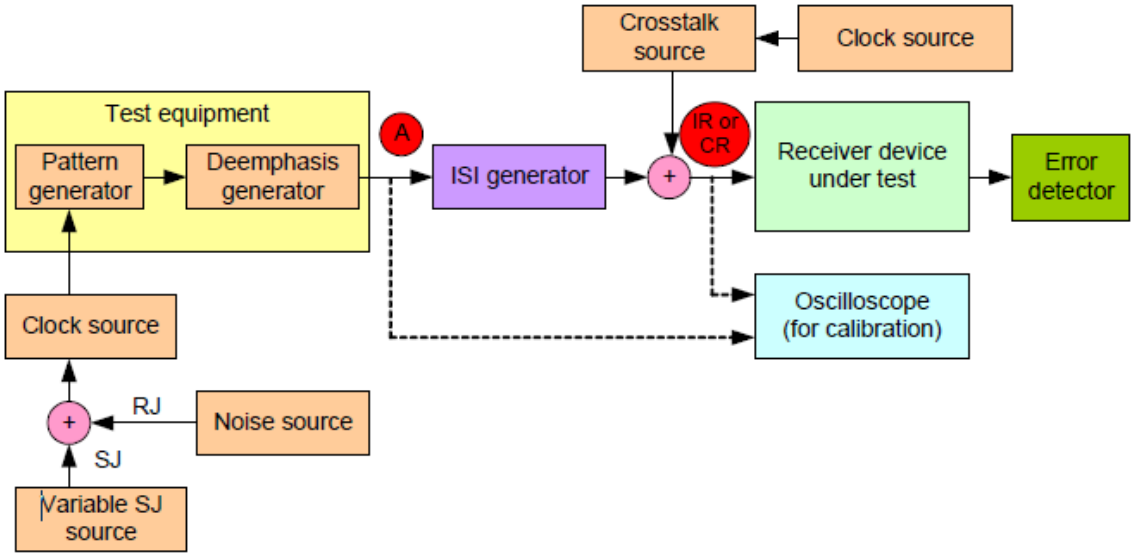


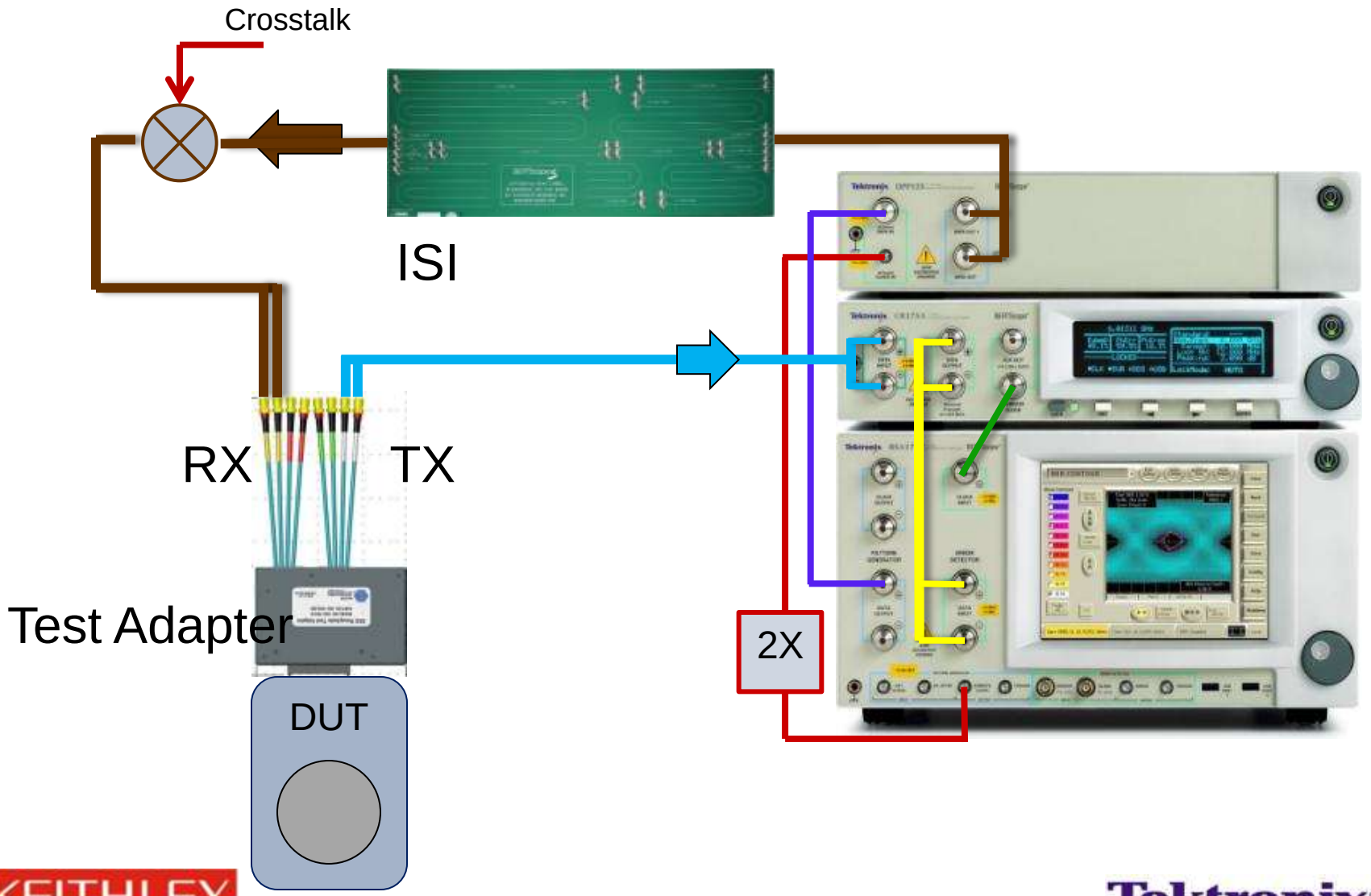

**Figure 129 — Stressed receiver device jitter tolerance test block diagram**

SAS 12 Gb/s Rx MOI

KEITHLEY
A Tektronix Company

Tektronix®

# SAS 12G Rx Equipment




KEITHLEY
A Tektronix Company

Tektronix

# Trained Link for Jitter Tolerance Test

- Complete Rx test exercises both CDR and Tx/Rx EQ capabilities
- Current options for training link
  - Iterate possible Tx/Rx EQ states and apply from 'best' optimized eye
  - Directly apply Preset based on typical configuration for worst case channel

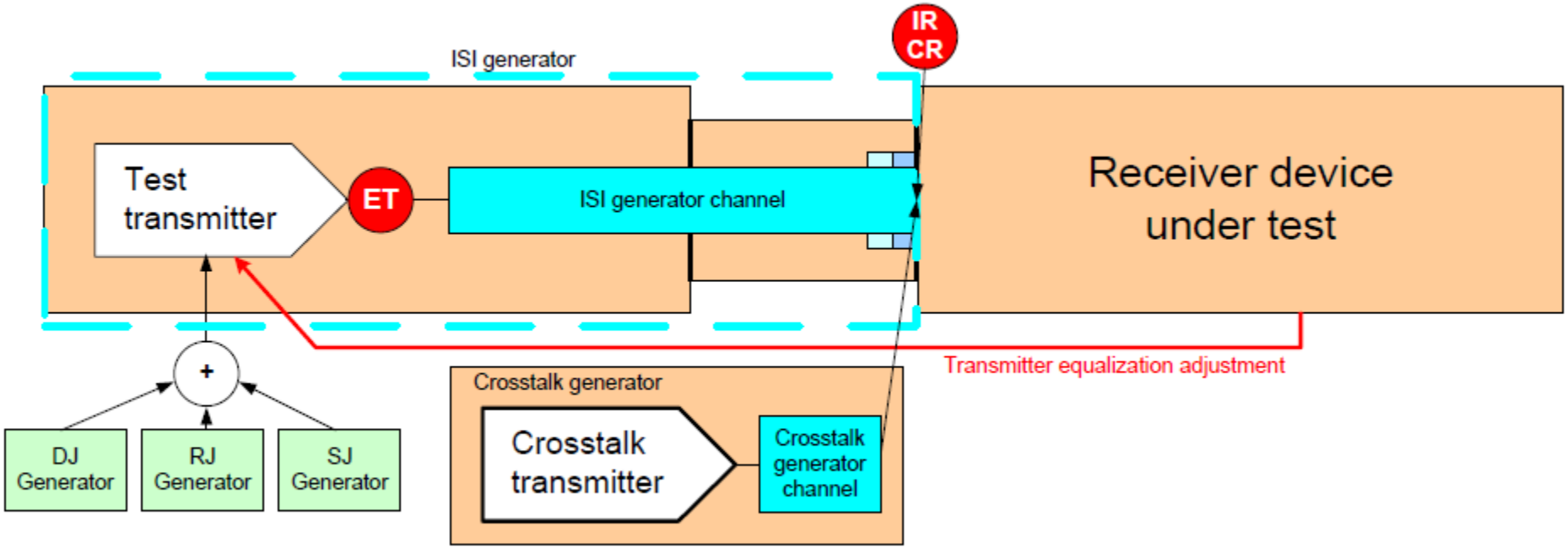
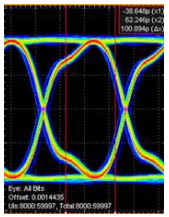


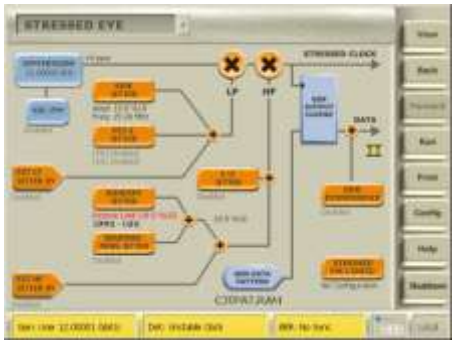

**Figure Fh – Stressed receiver transmitter equalization adjustment**

# Stressed Pattern Calibration – Putting it Together

***DPP125 Pre-Emphasis***

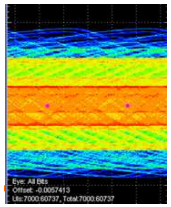
**1 Stressed Pattern Generator**



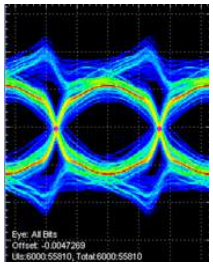


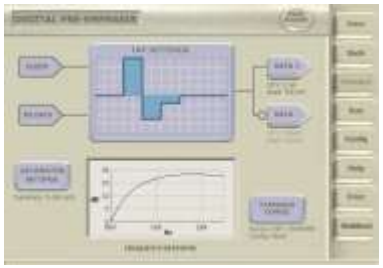
***BERTScope***

**2 Channel (crosstalk/ISI)**



***DPO/DSA72504D***





**3 Link Training**

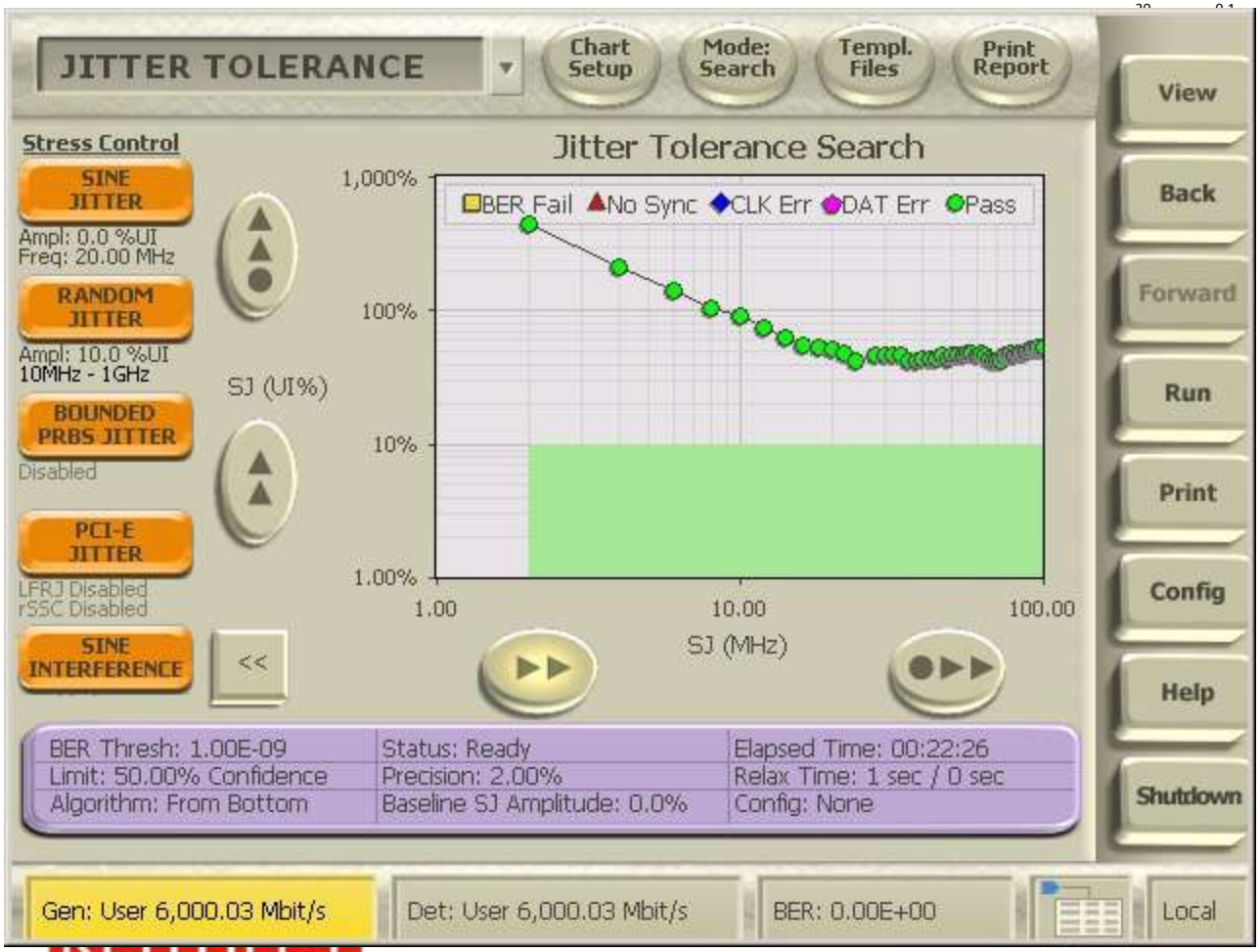
Physical Setup → RJ/SJ Calibration → ISI Calibration → Crosstalk Calibration → Tx/Rx Training → RX Testing

KEITHLEY
A Tektronix Company

Tektronix®

# Rx Results (BERTScope)

- Automated Scan from 10 Hz to 100 MHz
- SAS 12 Gb/s spec requires 97, 240 kHz & 2.06, 3.6 and 15 MHz




DATA

| T-MHz | T-SJ | SJ | Bits | Errors | BER | Status | ThreshVX | DelayPS |
|---|---|---|---|---|---|---|---|---|
| 2 | 0.1 | 4.52 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 267.531 |
| 4 | 0.1 | 2.1 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| 6 | 0.1 | 1.42 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| 8 | 0.1 | 1.04 | 6E+08 | 0 | 0.00E+00 | PASSED | -2 | 266.451 |
| 10 | 0.1 | 0.9 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| 12 | 0.1 | 0.74 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| 14 | 0.1 | 0.64 | 6E+08 | 0 | 0.00E+00 | PASSED | -2 | 266.451 |
| 16 | 0.1 | 0.56 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| 18 | 0.1 | 0.54 | 6E+08 | 0 | 0.00E+00 | PASSED | 1 | 266.451 |
| 20 | 0.1 | 0.52 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| 22 | 0.1 | 0.48 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| 24 | 0.1 | 0.42 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| 28 | 0.1 | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 267.531 |
| | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.42 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.42 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.44 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.44 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.44 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.44 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 267.531 |
| | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | -2 | 267.531 |
| | | 0.48 | 6E+08 | 0 | 0.00E+00 | PASSED | 1 | 267.531 |
| | | 0.48 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | -2 | 267.531 |
| | | 0.48 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.44 | 6E+08 | 0 | 0.00E+00 | PASSED | -1 | 267.531 |
| | | 0.42 | 6E+08 | 0 | 0.00E+00 | PASSED | -3 | 267.531 |
| | | 0.42 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.42 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | -2 | 267.531 |
| | | 0.48 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | -1 | 267.531 |
| | | 0.48 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.48 | 6E+08 | 0 | 0.00E+00 | PASSED | -2 | 267.531 |
| | | 0.48 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.5 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.52 | 6E+08 | 0 | 0.00E+00 | PASSED | -2 | 267.531 |
| | | 0.52 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | 0.52 | 6E+08 | 0 | 0.00E+00 | PASSED | -1 | 267.531 |
| | | 0.54 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 267.531 |
| | | 0.52 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | | | | LIMIT | | |
| | | 0.54 | 6E+08 | 0 | 0.00E+00 | REACHED | 0 | 266.451 |

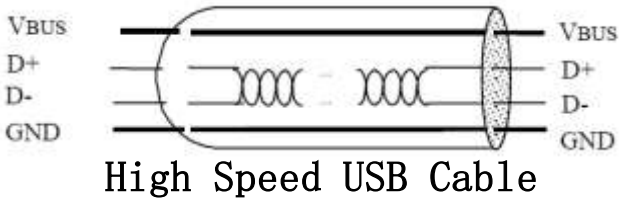
# USB3 – from 5Gpbs to 10Gbps

KEITHLEY
A Tektronix Company

Tektronix®

# Increasing Serial Data Bandwidth

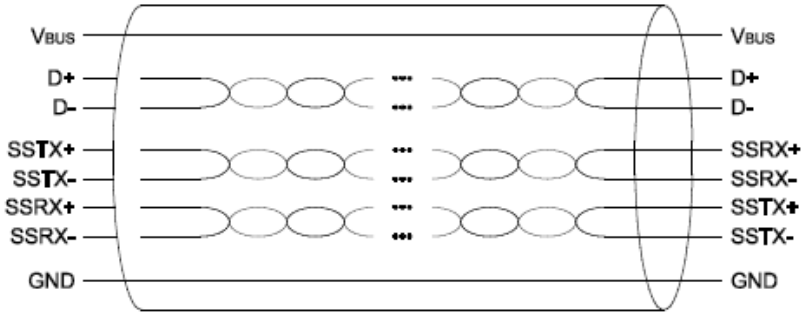
- **USB 2.0, 480 Mb/s** (2000)
  - Shift from slower, wide, parallel buses to narrow, high speed serial bus
  - 40x faster data rate, support for new connectors & charging



High Speed USB Cable

- **USB 3.0, 5 Gb/s** (2008)
  - ~10x faster data rate over 3 meter cable
  - Faster edges, 'closed eye' architecture

- **USB 3.1, 5/10 Gb/s** (2013)
  - 2x faster data rate over 1 meter cable
  - 'Scaled' SuperSpeed implementation



SuperSpeed USB Cable

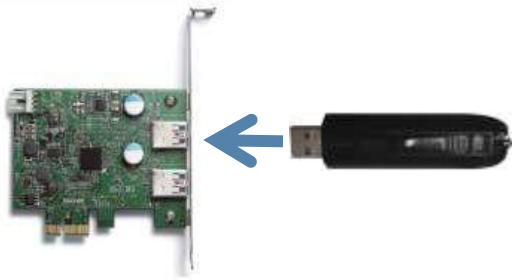
KEITHLEY
A Tektronix Company

Tektronix®

# Interoperability Challenge

- **Goal**: Any certified host works with any certified hub or device

- Short Channel
  - 1" host PCB route
  - ¼ " device PCB route
  - Direct plug



- Long channel
  - 4" host PCB route
  - 4" device PCB route
  - 1m cable

Source: USB-IF

KEITHLEY
A Tektronix Company

Tektronix®

# Why USB 3.1 is more challenging

| | Gen1 | Gen2 |
|---|---|---|
| **Data Rate** | 5 Gb/s | 10 Gb/s |
| **Encoding** | 8b/10b | 128b/132b |
| **Target Channel** | 3m + Host/Device channels (-17dB, 2.5 GHz) | 1m + board ref channels (-20dB, 5 GHz) |
| **LTSSM** | LFPS, TSEQ, TS1, TS2 | LFPSPlus, SCD, TSEQ, TS1, TS2, |
| **Reference Tx EQ** | De-emphasis | 3-tap (Preshoot/De-emphasis) |
| **Reference Rx EQ** | CTLE | CTLE + 1-tap DFE |
| **JTF Bandwidth** | 4.9 MHz | 7.5 MHz |
| **Eye Height (TP1)** | 100 mV | 70 mV |
| **TJ@BER** | 132 ps (0.66 UI) | 71 ps (0.714 UI) |

# USB 3.1 Transmitter Measurement Overview

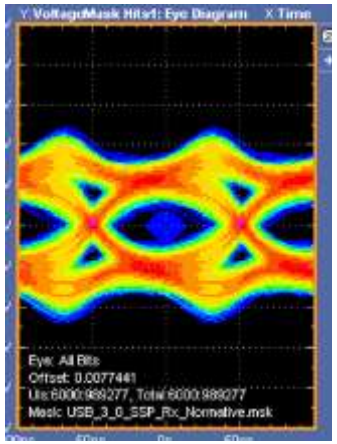
| Spec Reference | Parameter |
|---|---|
| Table 6-16 | SSC Modulation Rate<br>SSC Deviation |
| Table 6-17 | Unit Interval including SSC<br>Maximum Slew Rate (5 GT/s)<br>SSC df/dt (10 GT/s) |
| Table 6-17 | Differential p-p Tx Voltage Swing<br>Low-power Differential p-p Tx Voltage Swing<br>De-emphasized Output Voltage Ratio (5 GT/s) |
| Table 6-18 | Tx Min Pulse<br>Deterministic Min Pulse<br>Transmitter DC Common Mode Voltage<br>Tx AC Common Mode Voltage Active |
| Table 6-19 | Transmitter Eye<br>RJ/DJ/TJ - Dual Dirac at 10–12 BER |
| Table 6-28 | LFPS Common Mode Voltage<br>LFPS Differential Voltage<br>LFPS Rise Time<br>LFPS Fall Time<br>LFPS Duty Cycle<br>LFPS tPeriod<br>LFPS tPeriod-SSP (10 GT/s) |
| Table 6-29 | LFPS tBurst<br>LFPS tRepeat |
| Table 6-31 | LFPS tRepeat-0 (10 GT/s)<br>LFPS tRepeat-1 (10 GT/s) |
| Table 6-32 | LFPS Pulse Width Modulation (10 GT/s)<br>tLFPS-0 (10 GT/s)<br>tLFPS-1 (10 GT/s) |

**Clock**

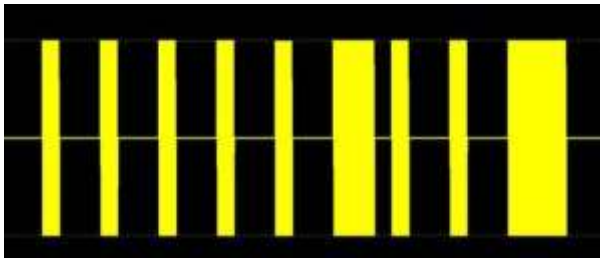
(CP10)

**PHY**

(CP9)*



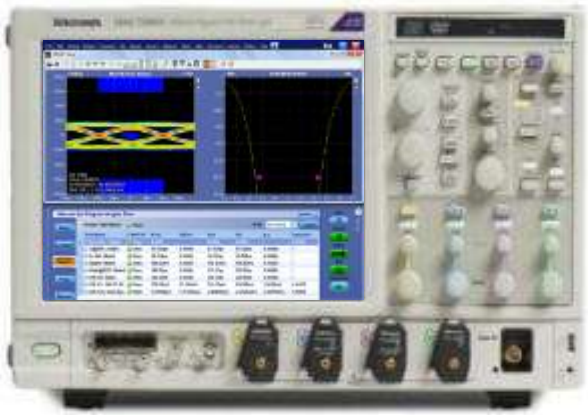

**LFPS**



KEITHLEY
A Tektronix Company

Tektronix®

# Example Host Test Setup



SMA cable to scope

Host

Ping.LFPS from signal generator (pattern toggle)

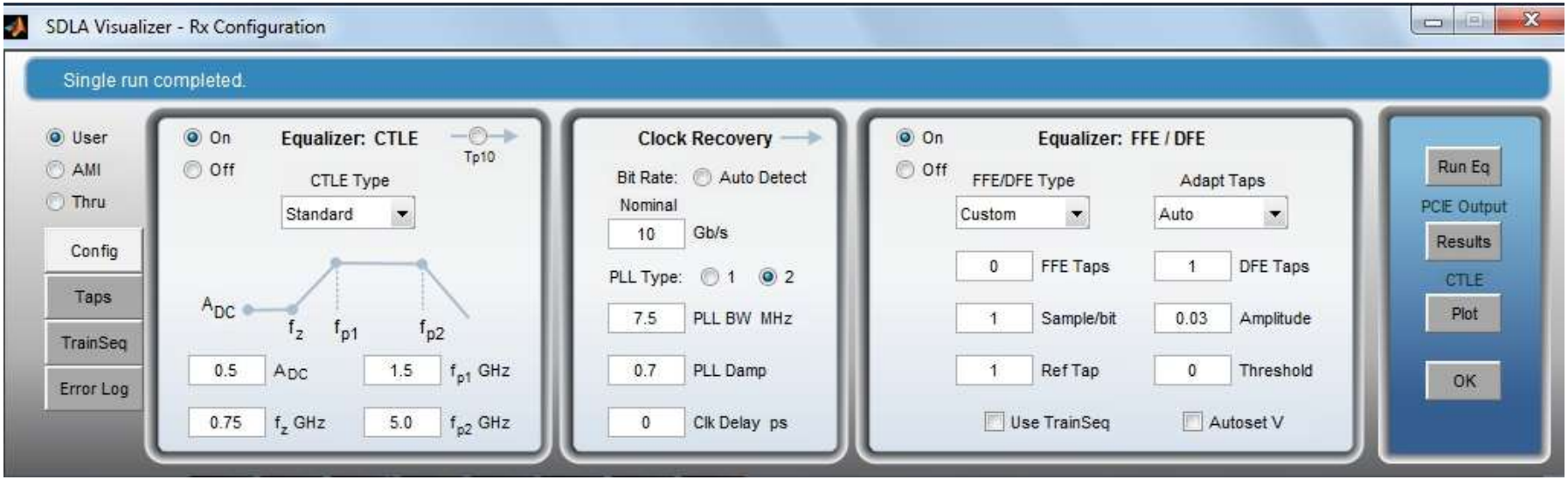
Short USB cable

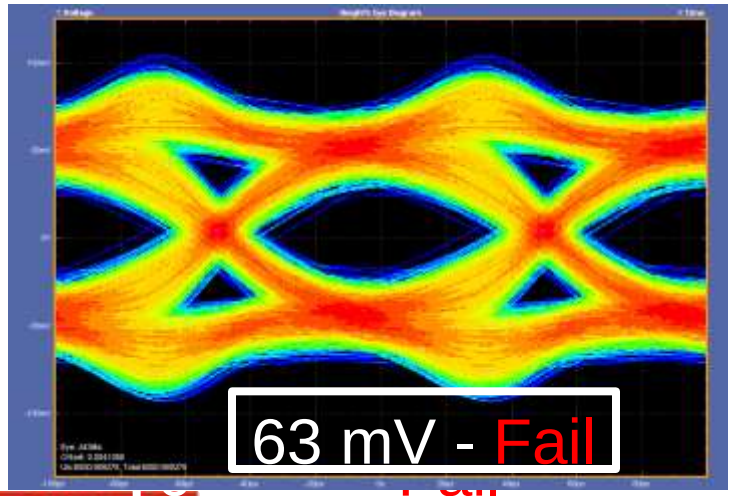
KEITHLEY
A Tektronix Company

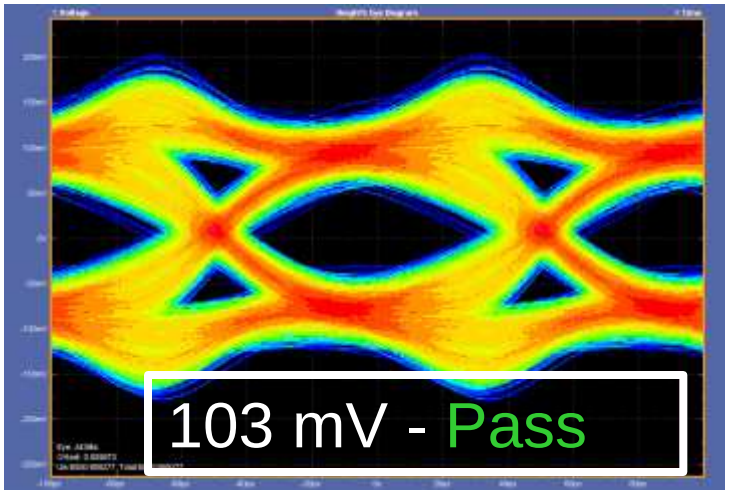
Tektronix®

# SDLA is critical for USB 3.1

- Find optimum Eye height vs. Rx EQ



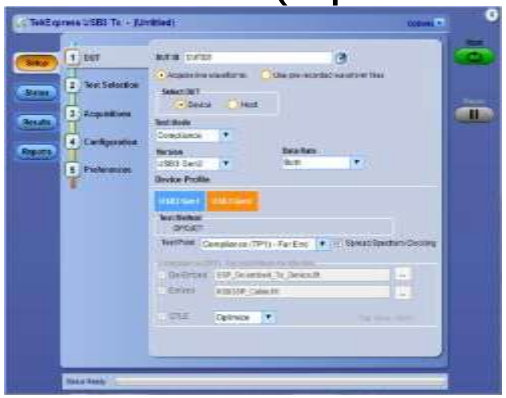




KEITHLEY
A Tektronix Company

Tektronix®

# USB 3.1 Recommended Transmitter Solution

- ≥ 20 GHz BW, 100 GS/sec preferred
- >10M minimum record length allows capture of 1M UI at 100 GS/sec, no interpolation.
- DPOJET for advanced jitter/eye analysis (Option DJA)
- SDLA for channel embedding and cycling through 7 CTLE/1 DFE settings (Option SDLA64)
- TekExpress automation software for USB 3.1 gen1/gen2 physical layer validation (Option USBSSP-TX)



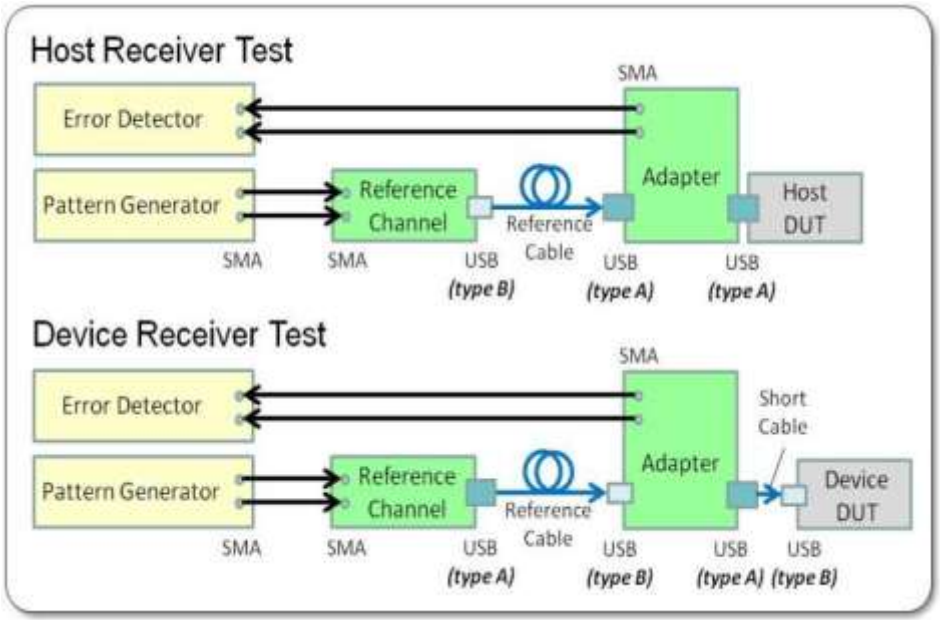
For instrument bandwidth, consider factors such as edge rate, reflections, SNR (de-embedding), and launch characteristics.

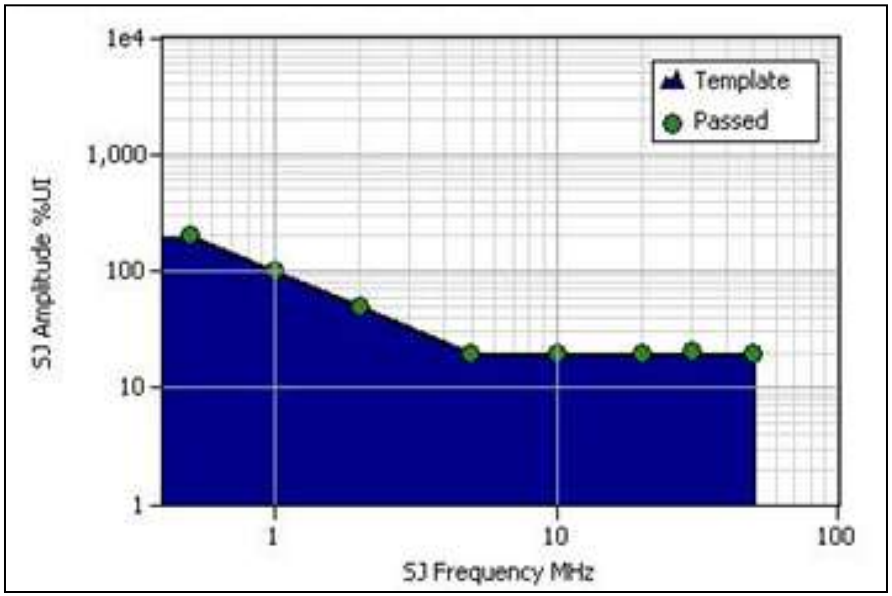
KEITHLEY
A Tektronix Company

Tektronix®

# Receiver Testing

- Jitter Tolerance (JTOL) with swept jitter profile, reference channel
  - Verify CDR tracking and ISI compensation
- Link optimization/training critical
  - No back channel negotiation
- Return “echoed” data to a BERT (loopback)
- Detected errors are inferred to be a result of bad DUT receiver decisions

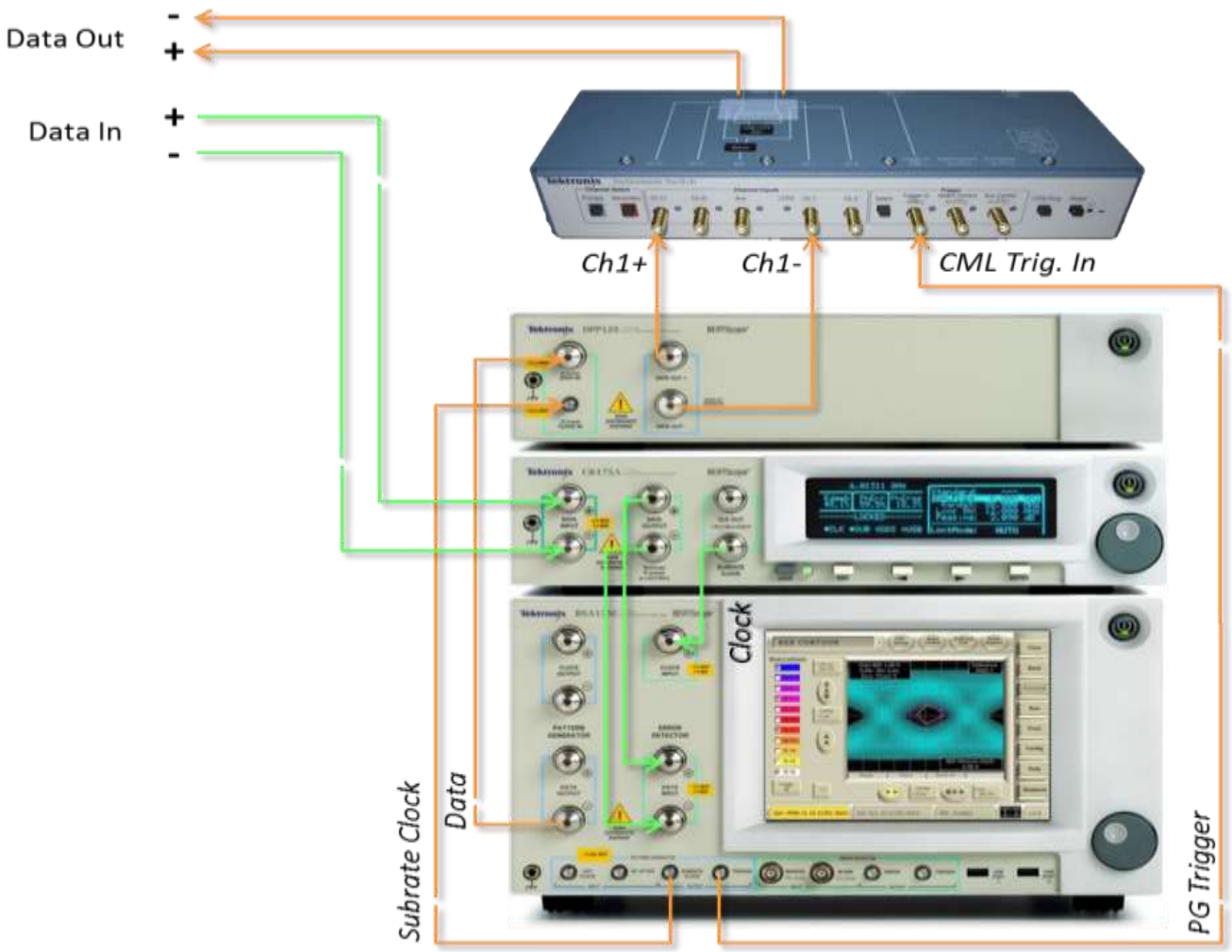



KEITHLEY
A Tektronix Company

Tektronix®

# BERTScope USB 3.0 RX Test Configuration




## USB Switch*

creates the low-frequency periodic signaling (LFPS) required to initiate Loopback-mode

## DPP125C
## De-emphasis Processor

## CR125A
## Clock Recovery

## BSA125C*
## BERTScope

KEITHLEY
A Tektronix Company

* Updates needed for USB 3.1 10 Gb/s

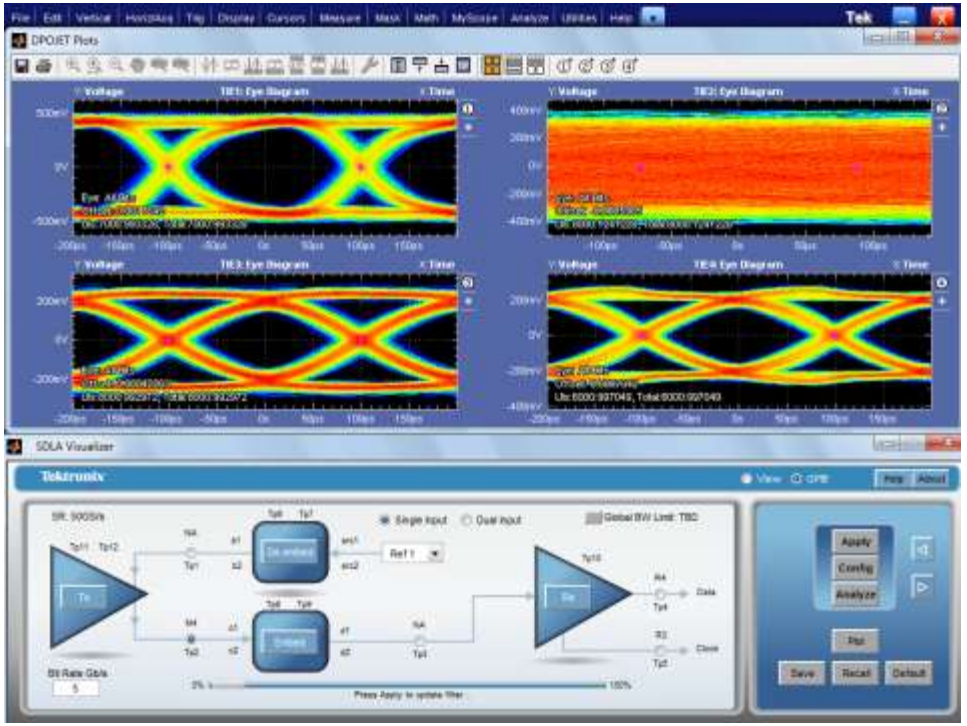
Tektronix®

# SDLA – Embed / De-Embed Simulation / Equalization


KEITHLEY
A Tektronix Company
Tektronix®

# Why use Link Analysis Applications?

- **Maximize Margins**
  Compensate for margin loss due to test fixtures, cables, probes or other artifacts of the measurement setup
- **Remove Reflections**
  Simulate probing at the ideal test point and remove reflections due to non-ideal probe locations
- **Open Closed Eyes**
  Apply receiver equalization to compensate for channel loss before analysis
- **Compliance Test**
  Validating DUT for standards that require de-embedding, channel embedding, and equalization



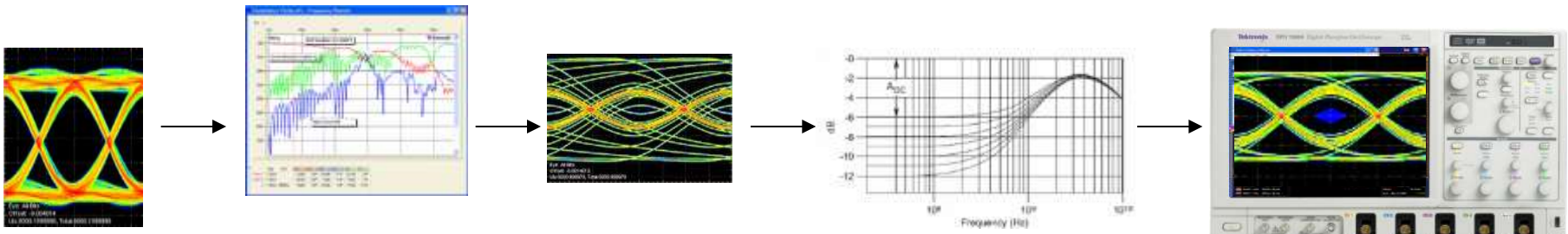

KEITHLEY
A Tektronix Company

Tektronix®

# Open Closed Eyes

## *Apply Receiver Equalization*

- In the past, acquired signals could be measured directly, even at the far end
  - Increasing data rates require some level of equalization to compensate for channel loss at the transmitter and/or receiver
- Standards, for example, PCI Express 3.0 specify a reference equalizer that must be used during compliance testing
- PCI Express uses a CTLE + 1 Tap DFE
  - CTLE parameters and DFE tap value are optimized to produce the largest eye area based on the transmitted signal and channel



**Signal Acquired from Compliance Board**

**Embed the Compliance Channel**

**Closed Eye due to the Channel**

**Apply the Optimized CTLE + DFE**

**Open Eye for Measurements**

KEITHLEY
A Tektronix Company

Tektronix®

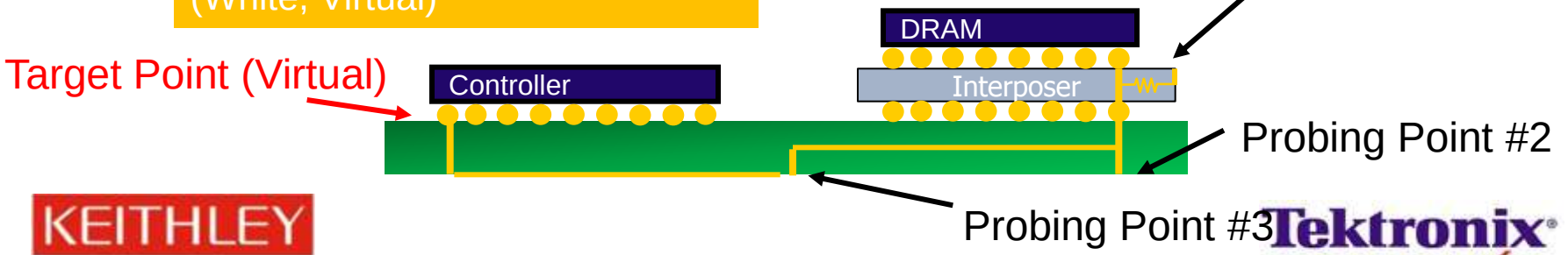
# Remove Reflections

## *Virtual Probing at Ideal Test Point*

- Reflections may be present when probing at non-ideal locations, which are not present at the ideal test point
  - Measure signals at controller side from memory side
    - BGA interposer (#1) or vias under memory chip (#2)
  - Measure both controller and memory side signals from midbus probing (#3)

Waveform at probing point (Purple, Actual)

Waveform at controller side example. removing reflection (White, Virtual)




KEITHLEY
A Tektronix Company

Tektronix

# Tektronix HDMI 2.0 Solution

- **DPO/DSA/MSO 70004B/C/D/DX Series Real Time Oscilloscope with BW ≥ 16GHz ( we also support 12.5GHz BW scope for HDMI 2.0) with Opt 10XL, Opt DJA, Opt SR-EMBD and SR-CUST.**
- **HDMI 2.0 Advanced Analysis and Compliance Software for Source– Option HDM ( will need Opt HT3 as HDMI 1.4b testing is a pre-requsite for HDMI 2.0)**
- **HDMI 2.0 Advanced Analysis and Compliance Software for Sink- Option HDM-DS ( this needs Opt HDM and will need Opt HT3-DS as HDMI 1.4b testing is a pre-requsite for HDMI 2.0).**
- **Probes – P7313SMA (Four) ( If less probes are used, offer TF-HDMI-TPA-T-termination board)**
- **HDMI 2.0 Test Fixture – Available from Third Party.**
- **HDMI Termination board (TF-HDMI-TPA-T)**
- **AWG70002A with Opt 01,03 and 225 ( Qty.2) OR AWG7122C with Opt 01,02 or 06 and 08 for the innovative direct Synthesis based HDMI 2.0 Sink Testing.**
- **DSA8200 or Equivalent with 80E03/80E04 and I-Connect Software for MHL cable testing ( performed manually using MOIs)**

**Please contact local Tektronix account managers for further details.**

KEITHLEY
A Tektronix Company

Tektronix®

# Tektronix MHL Solution:
# Complete Solution for Phase 1 CTS 3.0 needs

- Tektronix MHL Physical Layer Tx test setups are easy to use and automated **( OPT MHD3)**
  - Simple test setups common for most tests
  - Vterm provided by scope itself
  - MHL Fixtures available from our Fixture partner Wilder Technologies
- Tektronix MHL Physical Layer Rx test setups are easy to use**.( Manual testing for Phase 1 CTS needs)**
- TRUE MHL SIGNAL Generation as there is no need for external combiners/Filters
  - No need for external ISI boards as we leverage our AWG direct Synthesis Capability with common setups for Sink and Dongle testing
- Tektronix also offers complete MHL solution with:
  - DSA8200 or Equivalent Sampling scope with 80E03/04 and I-connect Software for MHL Cable testing (performed manually using MOIs)
  - Low Bandwidth Oscilloscopes
  - Keithley Source Meter (Now part of Tektronix)
  - Programmable Power Supply and
  - Digital Millimeter



KEITHLEY
A Tektronix Company

Tektronix

Tektronix

# Thanks !

KEITHLEY
A Tektronix Company

Tektronix